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Technical Briefs

Marvels of Microelectronic Technology: From the Floating Gate and Charge Trapping concepts to the Flash Memory of Terabit class

by Simon Deleonibus, Past Chief Scientist CEA, LETI

Introduction

In this Technical Brief, we are focusing on the discovery, inventions and development of modern Non Volatile Memories (NVMs). Whereas, we reported on the invention and development of Dynamic Random-Access Memory (DRAM) in the October 2019 Newsletter issue.

Since the years 1990s to 2000s, NVMs, in their Flash Floating Gate and Charge Trap (FFG&CT) versions, have become the market and technology driver for integrated circuits as they entered the mass market through the camera, automotive and, further on, communication markets. Who among us has not used a USB key, a Solid State Disk (SSD), stored data on a mobile phone, or used a digital camera? No one can ignore today the formidable expansion of FFG&CT NVMs and the way they overcame the leadership on DRAM and Logic circuits as technology driver for Nanoelectronics. NVMs have gone through the highest number of conceptual and architectural changes in the past 50 years, evolving at the same time, from a niche product to a mass production driver. Just to give an example, Multi-Deca Gigabit (several tens of Gbit) USB keys, based on FFG&CT organized in a NAND architecture, are *given almost for free* nowadays as a *storage and code share vector.* Whereas, 256k NOR Erasable Programmable Read-Only Memory (EPROM), which were necessarily erased by using a UV lamp, were used for professional applications, essentially for storing microcontroller programs in the 1980s! Many hurdles have appeared in their 2-dimensional (2D) scaling, and today 3-dimensional (3D) multilevel cells (up to 4bits/cell) integration can increase the bit density without requesting conventional device scaling. The NAND FFG&CT memories have reached the Terabit integration level, using either an intermediate floating gate or pseudo floating gate charge trapping. Their market exceeded $52B in 2018, which is unprecedented. They are on the way

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Marvels of Microelectronic Technology: from the Floating Gate and Charge Trapping concepts to the Flash Memory of Terabit class

(continued from page 1)

to replacing hard disk drives (HDDs) in computers and equipping data centers with Solid State Disks (SSDs).

Two major key persons that marked the history of Non Volatile Memories research and development, Professor Simon M. Sze, NCTU, IEEE Fellow, IEEE EDS Celebrated member (Figure 1a) and Professor Fujio Masuoka, Tohoku University, IEEE Fellow (Figure 1b), have kindly accepted to testify on the birth of the discovery of the floating gate effect and the invention of Flash Memories, respectively. Their testimonies are reported in sections 1 and 2. In section 4, members of the former team at Toshiba Memory (spun into Kioxia) who invented and first announced the 3D BICS-FLASH™ architecture graciously accepted to share their recollection.

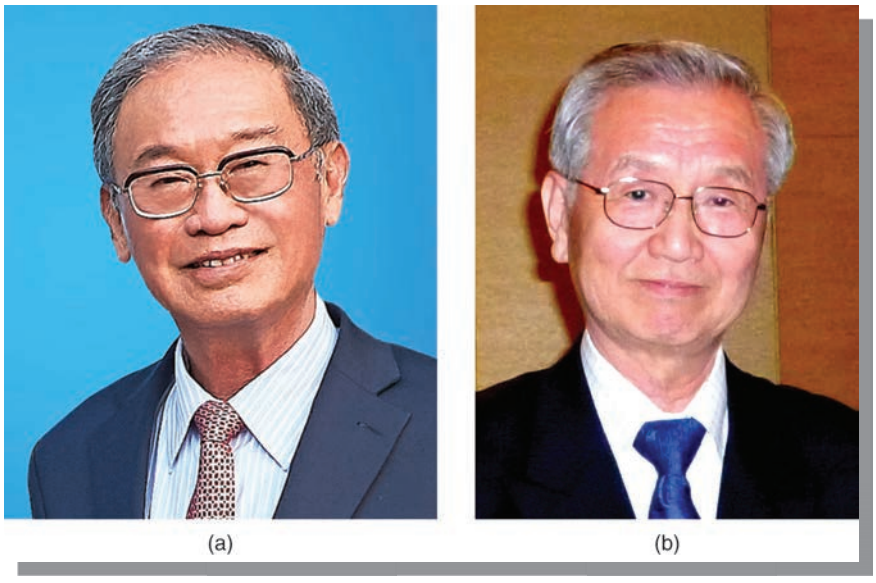

Figure 1 Recent portraits of: (a) Simon M. Sze (by courtesy of Simon Sze) (b) Fujio Masuoka (by courtesy of Fujio Masuoka)

1. Simon Sze and the early cradle age of Floating Gate memories

Everybody in the semiconductor business knows Professor Simon Sze for his very popular and authoritative books, discoveries and inventions. The author of this Technical Brief accompanied his learning of semiconductor devices as an undergraduate student through Simon Sze's book titled ***Physics of Semiconductor Devices*** [1], first published in 1969, and is still using it daily as a reference just as many other scientists and engineers worldwide. Among the many seminal discoveries, inventions, studies and papers that Simon Sze authored in his career, the co-discovery of the Floating Gate Memory effect has certainly brought a revolution in our business and changed the societal way of living worldwide. Dawon Kahng and Simon Sze, Bell Labs researchers at that time, published a seminal paper in the Bell System Technical Journal in June 1967, in which they explained the Floating Gate Memory (FGM) effect [2]. The device featured a 50 Å SiO_2 gate oxide, 1000 Å Zr floating gate, 1000 Å ZrO_2 coupling insulator and an Aluminum control gate. Pulses at 50 V and 0.5 μs were necessary to inject charge through the gate oxide from the Insulated Gate Field Effect Transistor (IGFET) channel into the floating gate, by capacitive coupling between the control gate and the floating gate (Figure 2a). Depending on the insulator, the charge injection (Figure 2b) was believed to be due to a Fowler-Nordheim (for example in SiO_2 or Al_2O_3) or Poole-Frenkel (Si_3N_4) mechanisms.

This was the very beginning of 60 years in research and development on the basic principle of charge storage/trapping in a stacked gate (1 control gate and 1 floating gate) device, and neutralization of the charge by an erasure mechanism, for example by applying an opposite voltage on the control gate. Without naming it explicitly, Kahng and Sze believed that such a device was announcing the Electrically Erasable Programmable Read-Only Memory (EEPROM). Many options and many divergent interests existed around the table without a dominant application really emerging at the beginning.

Since then, the Floating gate memory cell has proven to be the smallest memory device based on one transistor. It has beaten all predictions after being unrecognized or criticized as being expensive to make, unreliable and incompatible with logic devices, due to high program/erase voltages, and thus necessarily using a thick gate oxide susceptible to being stressed and suffering from induced defects. Nowadays, on the contrary, it has become a commodity product offering programmable/erasable mass storage media after 50 years of continuous struggle and studies.

In the frame of our exchanges, Prof. Simon Sze explained the motivations that led him and D. Kahng to invent the floating gate device for memory applications: *"In the*

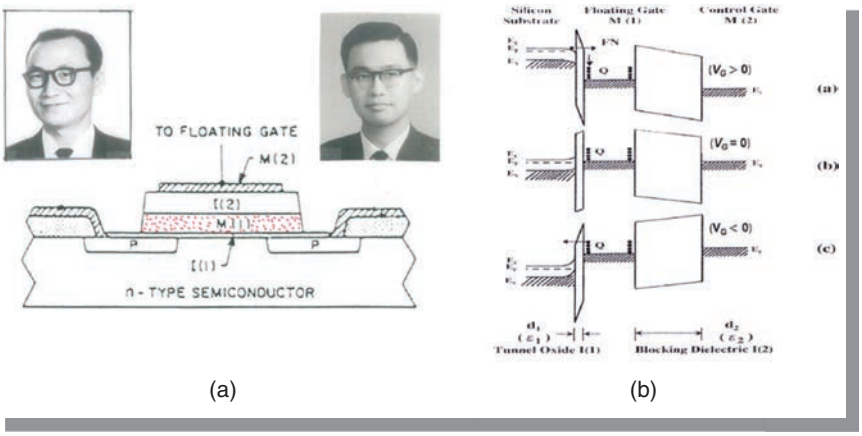

Figure 2(a) First floating-gate memory (FGM) by Dawon Khang (left) and Simon Sze (right). (Courtesy of Simon Sze) and Figure 2(b) Band diagram of a Floating gate transistor structure during: (a) charge trapping,(b) storage and (c) detrapping (discharging) (Courtesy of Simon Sze)

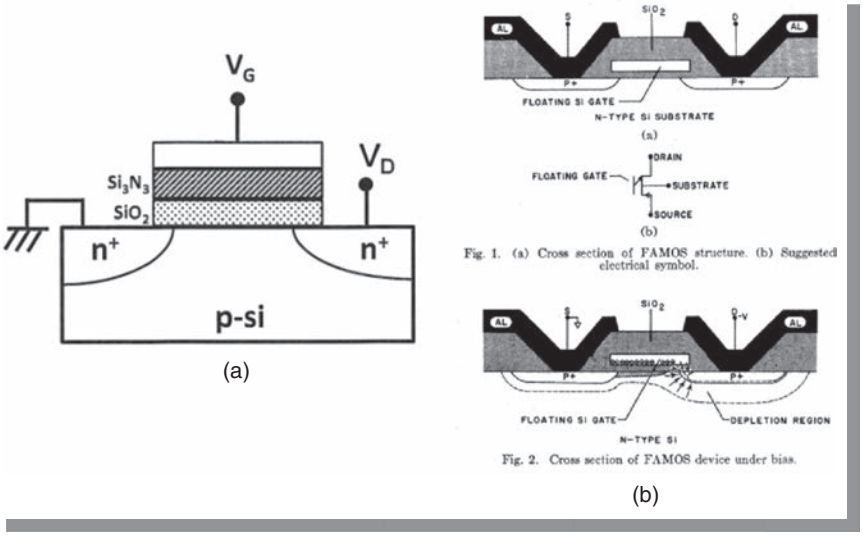

Figure 3(a) MNOS structure (Wegener et al.): discrete charge trapping devices (Courtesy of Simon Sze) and Figure 3(b) Floating gate Avalanche-injection MOS (FAMOS) structure [6]

mid 1960's, magnetic core memory (MCM) was used in computers. It took a long time to turn on the mainframe computer (m/c). We thought a semiconductor memory should be faster than the MCMs to boot up the mainframe computer (m/c)." Simon Sze adds: *"When we submitted our paper to BSTJ in May 1967, we really did not know that FGM would eventually supersede all prior non-volatile memory technologies (e.g. magnetic tapes, HDDs, optical disks) and in early 21st century ushered in the 4th Industrial Revolution and brought unprecedented benefit to the mankind.*" The paper introduced not only the basic concept of non-volatility in semiconductor devices, but also the floating-gate structure which is still the dominant technology for nonvolatile information storage.

In those days, many engineers and researchers wanted to use Read Only Memories for code storage by an electrical action, without necessarily being able to erase and program again. That is why the devices were pointed out as "alterable memories". Coincidentally with Kahng and Sze's discovery, in December 1967, H.A.R. Wegener from Sperry Rand Research Center published research on the Metal, Nitride Oxide Silicon (MNOS) transistor [3] in which charges were stored in silicon nitride layer traps by the Poole-Frenkel transport, after injection through the underlying tunnel oxide (Figure 3a). It resulted in a memory device with low charge retention capabilities, due to leakage through the gate. Other authors reported similar structures [4]. Keshavan and Lin reported on the band gap engineering of the insulating stack by introducing an extra oxide layer between the gate and channel, resulting in a MONOS structure [5]. The extra layer avoided charge leakage from the nitride to the gate and modified the transistor threshold voltage as well.

From the 1960's to the beginning of the 1970s, only mask writable memories (Read Only Memories or ROMs) were available. Electrically programmable/erasable devices were still confined in their infancy. In 1971, Intel proposed a 2kBit Floating gate Avalanche-injection MOS (FAMOS) memory [6], without a control gate, to store charge from the MOSFET drain (Figure 3b) by using a carrier injection from the avalanche current at the drain. Pulses of 50 V for 5 ms, with a load current of 50 mA, were necessary to program 1 bit. The memory was UV erasable collectively but still needed to be programmed bit by bit, due to its NOR gate architecture. However, the absence of a control gate could not make it electrically erasable.

2. The advent of Flash memories

Fujio Masuoka was an intellectually precocious child, especially good at math, had overwhelming capacities by three years in advance at the school and high school levels. He was thus a very curious spirit and certainly keen to taking risky paths for innovation. Early

in his career at Toshiba, he worked on DRAM as a development engineer as well as a salesman.

At that time, Ultraviolet (UV)-EPROM and EEPROM were available. However, there were cost per bit issues with UV-EPROM and EEPROM. EEPROM needed a much more complex architecture (two transistors) than UV-EPROM, which were more compact and scalable. However, UV-EPROMs posed more constraint at the system level (UV collective erasing) and made them less popular.

"*My idea on EPROM was that programming can be performed at a lower voltage and a higher speed than that of the conventional EPROM, by using a control gate. In the invention USP 3,825,945 I claimed that the capacitance between the floating gate and control gate should be larger than that between the substrate and floating gate* [7]" says Masuoka. An increased coupling ratio (ratio between the control gate/floating gate capacitance and floating gate/substrate capacitance) resulted in enhanced charge injection into the floating gate from the device channel. Moreover, Masuoka and Iizuka proposed to use stacked polysilicon electrodes separated by a coupling insulator to implement the control and a floating storage gate [8–10], in a one transistor cell programmable in a drain avalanche mode. The Stacked-gate Avalanche-injection MOS (SAMOS) memory established a direct link with polysilicon gate CMOS, which was becoming the mainstream technology (Figure 4a). These conditions, put together, formed the concept for a future commodity-like product that was never thought, but finally proven to be capable of competing with DRAM in terms of density and cost per bit, even though not as fast. The success of the digital cameras, of the flexibly mobile mass storage in the form of USB keys, and of mobile phones, boosted the demand for such devices easily usable by the public at large. This demand was enabled by Flash Memories. However,

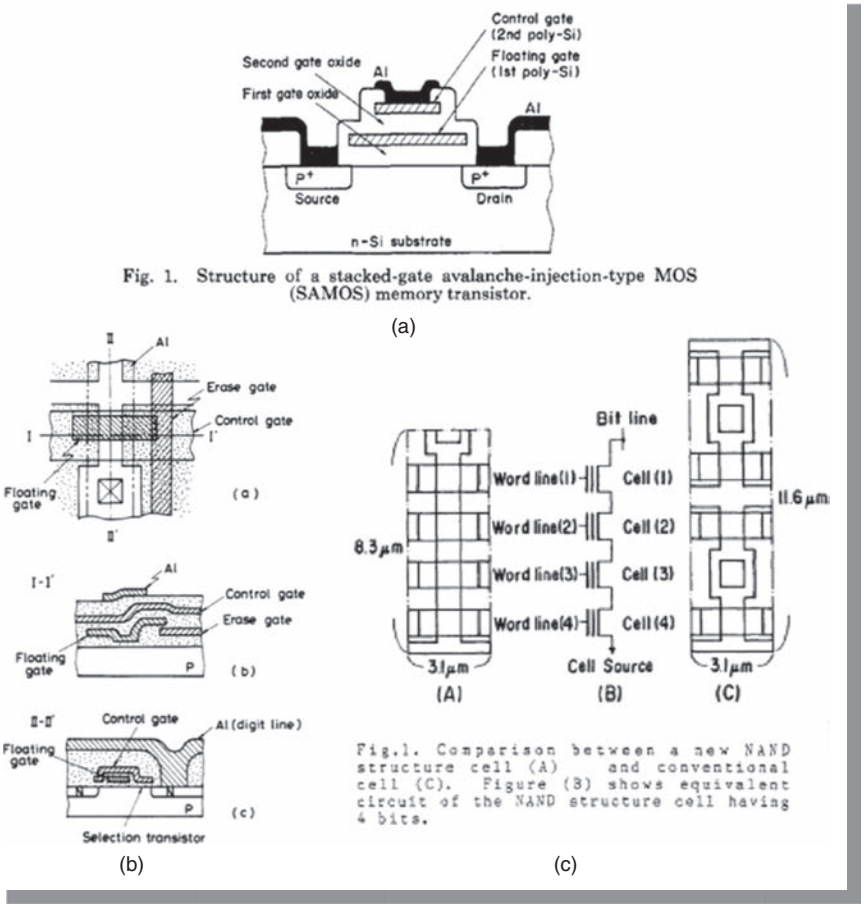

Figure 4 (a) SAMOS structure [9] programmable by charge injection resulting from drain avalanche breakdown and electrically or UV erasable—partially presented at IEDM 1972 late news; (b) First paper on Triple poly Flash Memory (NOR gate), presented at IEDM 1984 [12]; (c) First paper on NAND type Flash Memory, presented at IEDM 1987 [15]. Comparison between NOR and NAND gates layout. will be details of Fig.4b visible after printing?

at this point, still the "battle was not won"!

In the early 1980s, the EEPROM required two transistors per bit (a non-volatile memory transistor and a select transistor) necessarily bit by bit rewritable. How could each bit be reduced to one non-volatile memory transistor only to reduce the bit cost? "*The cost per bit could drop much lower to a quarter,*" declares Masuoka who paradoxically underlines: *"I noticed that by erasing all bits at once, and then writing bits on a per-bit basis, a select transistor would not be needed. This marked the advent of electrically-rewritable Flash Memory, which can be erased all at once, with only one non-volatile memory transistor for each bit, granted as USP 4,437,174* [11]." This conclusion was counter-intuitive even for many professionals because erasing all bits in a sector to change one was seen as a "waste of time". The erasure was obtained by injecting electrons by field emission between the control gate and a third polysilicon erase gate. Actually, at the small scale of writing/erasing times, collective Flash erasure was not an issue and was energy wise efficient. The working principles behind NOR flash memory were presented at the 1984 IEDM [12] (Figure 4b), and 256-kbit NOR flash memory was announced at the 1985 ISSCC [13].

Masuoka adds: *"In 1986, I eventually noticed that NOR flash memory was so insufficiently low cost that it could not drive out magnetic disks, and that the Flash Memory should be needed to further reduce the cell area*

per-bit. The answer was NAND Flash Memory, granted as USP 5,245,566 [14]. In April 1987, I successfully verified the basic properties of the NAND flash memory, namely writing, reading and erasure by bulk injection." The results were presented at the 1987 IEDM [15] (Figure 4c)

Masuoka wanted to quickly prototype a 4Mbit NAND Flash circuit, but had a hard time to convince his management to provide mask funding. He failed to get any funding from the computer division, because they found the concept too ambitious to replace magnetic storage memories.

"If I'd given up there, all my work up to then would have come to nothing," confesses Masuoka. He found an ally at the Consumer Electronics Division to financially support his project: *"I explained to Mr. Tajiri, Director of the Consumer Electronics Laboratory, that if we managed to produce 4-Mbit NAND flash memory, cameras would no longer need film. I was indeed explaining that the digital cameras which we know today would become possible. We successfully developed 4-Mbit NAND flash memory in 1988 and announced 4-Mbit NAND flash memory at the ISSCC in February 1989* [16]. *Thereafter, Mr. Tajiri used the 4-Mbit NAND Flash memory to launch the world's first digital camera to replace conventional film with NAND flash memory. At the time, the price of the flash memory was high and the world's first flash memory-based camera didn't sell well."*

Masuoka finally concludes: "*Now, Flash Memory is penetrating into the whole economic framework. The world-wide market size of the NAND Flash Memory last year surpassed $52B. In the near future it is expected to become more than $100B, which is unmatched in the history of the world, when all the HDD's in the personal computers are replaced by the SSDs, and the HDD's of the data station of Google and FaceBook, etc. are partially replaced by the SSDs. This is because the market share of not only the semiconductor memory but also the HDDs is accounted. And also, many power stations in the world can be saved by replacing the HDD by the SSD. For this is what the final target of the NAND Flash Memory is all about, and there is no doubt at all that the NAND Flash Memory is an earth-conscious 'Green Technology'.*"

3. Looking for new breakthroughs in process integration

At the beginning of the years 2000, the quest for an efficient solution to increase the capacity of floating gate based Flash Memories beyond the 70–50 nm node has been an ongoing question. As a matter of fact, the high voltage used for cell programming/erasing and the floating gate architecture itself, imposed insulators thicker than for logic devices to withstand the reliability constraints. Such a situation made the floating gate transistors more sensitive to short channel effects and to a retention and endurance degradation due to Stress Induced Leakage Current (SILC). Cell to cell disturbance increased with spacing reduction. At such a point, several alternatives were making sense to move aside the necessity of 2D linear scaling to increase memory capacity. Beyond stacking 2D memory arrays in a package, other device architecture or integration based solutions were being developed. One idea was to increase the number of bits per cell [17] by programming several states corresponding to several threshold voltages to read, the limit being the threshold voltage distribution variability and the associated noise margins. Nowadays, up to 4 bits per cell are implemented in large capacity SSD circuits (see hereunder). Another way was to stack 2D arrays at the chip level [18], with a limit in a cost per bit reduction approach.

Finally, a multiplication of vertical 3D strings Flash architecture was proposed by Toshiba [19] by the so called Bit Cost Scalable (BiCS) technology, renamed BiCS FLASH™. The vertical gate-all-around transistor architecture with discrete traps (pseudo floating gates) storage had a higher electrostatic integrity than the conventional 2D architecture. Moreover, the vertical gate-all-around structure did not require such aggressive lithography capabilities to increase the final circuit capacity and resulted in a highly competitive cost per bit.

4. Three Dimensional (3D) Flash Memory: BiCS FLASH™ at TOSHIBA's memory division[1]

At Toshiba, the BiCS FLASH™ technology was developed as soon as July 2005 when the first idea came out. Toshiba announced the first example of a vertical channel based high density Flash memory array, featuring gate all-around transistors and a SONOS like gate stack structure. As in all major memory companies, there were discussions on different options to solve the scaling issues of 2D Flash Memories: an increasing transistor variability, a program disturbance due to neighboring cell interferences, and an increasing fabrication tools cost. Options such as 3D stacked floating gates, FeRAM, ReRAM, PCRAM were being considered in the discussion. In that context, a cross-point architecture was published by Matrix Semiconductor (now Sandisk), composed of cross-bar type one-time programmable memory cells, stacked repeatedly [20]. At that time, Hideaki Aochi was leading a non volatile memory process integration team at Toshiba. Note that the company has recently spun off its memory business by creating KIOXIA.

Aochi, now a KIOXIA engineer, recalls: *"The cross point architecture needed a large number of process steps, because of the large number of repetitions of the similar cross-bar shaped memory structure. A large fabrication chip cost was a severe issue."*

[1] Currently spun off from Toshiba and renamed as KIOXIA.

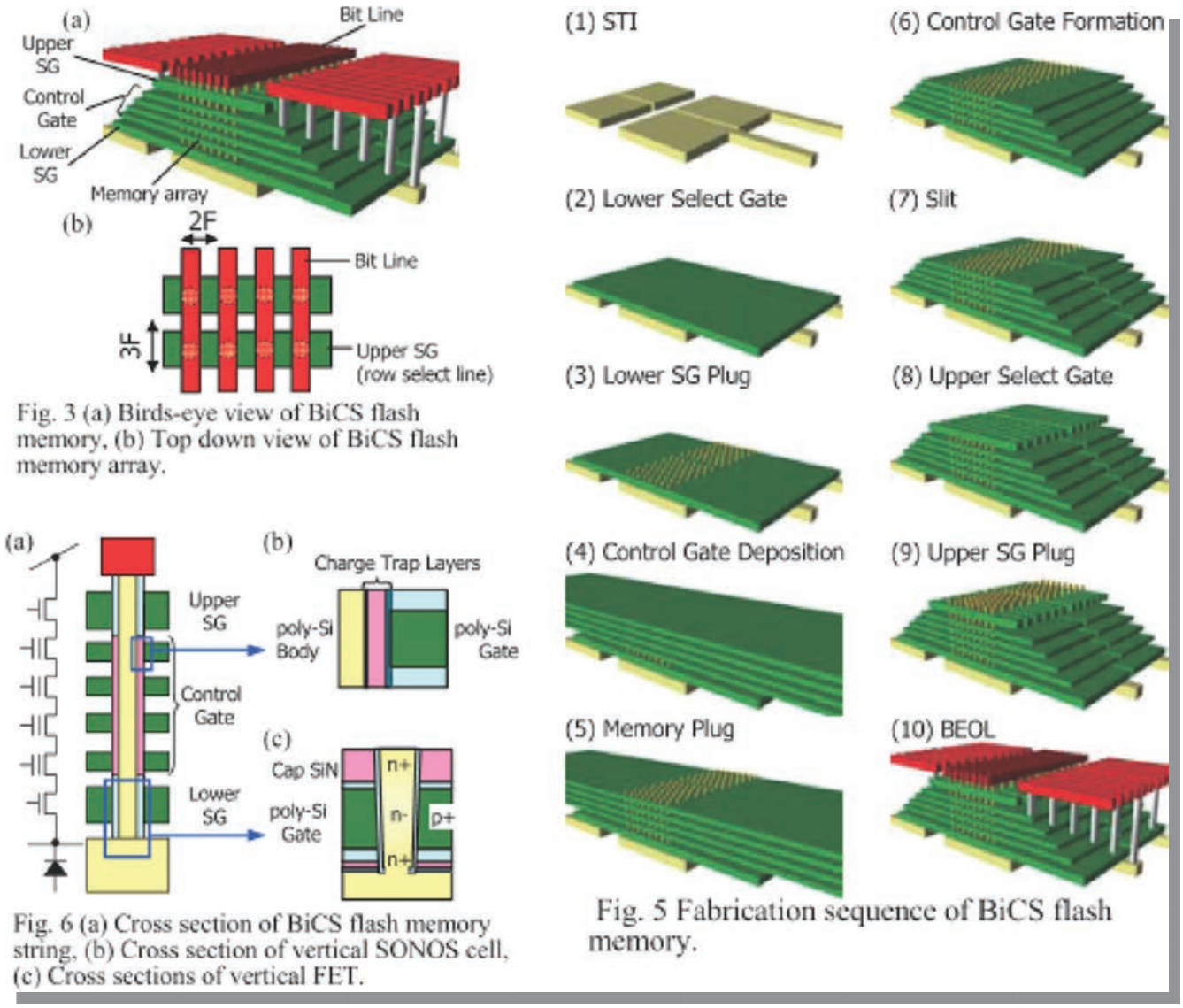

Fig. 3 (a) Birds-eye view of BiCS flash memory, (b) Top down view of BiCS flash memory array.

Fig. 6 (a) Cross section of BiCS flash memory string, (b) Cross section of vertical SONOS cell, (c) Cross sections of vertical FET.

Fig. 5 Fabrication sequence of BiCS flash memory.

Figure 5 First publication of the BiCS FLASH™ Memory technology at VLSI Technology Symposium in June 2007 [19].

Aochi remembers: *"One day, during my ride in the commuter train, I had gotten the basic idea of punch and plug process to make a hole thru many stacked layers of two different materials. Then our team had started to construct all the elements of the basic concept of BiCS FLASH™, which are: detailed process integration, device design, array structure, staircase layout, and row/column wiring connection to driver and sensing circuit." (Figures 5, 6).*

Many questions arose while starting to implement such a seductive idea: the impact of a polysilicon channel on variability and the process integration of a vertical gate-all-around transistor. Since the 1980s, at the time of advent of thin film p-channel transistors load for Static RAMs or displays row- and column-select transistors, the use of polysilicon channels in the fabrication of logic or memory circuits of ULSI densities was highly challenging and many questions existed around on a possible variability issue. These types of devices were better known in the field of displays but for much larger geometries.

Aochi says: *"After some experiments, we realized that the variability of transistor performance had been caused by two major factors, one was due to the poly-Si channel, as we had expected, and the other was the contact resistance of the connection of the poly-Si channel to the substrate."*

The solution was to give a hollow tubular shape to the memory strings and to thin down the polysilicon channel to keep electrostatic integrity, just as in a thin body SOI transistor. Typical macaroni shaped channels were thus implemented. A pipe-shaped string structure could eliminate the bottom contact of the poly-channel

Figure 6 Members of the BiCS FLASH™ Memory team celebrated at KIOXIA. From left to right: (Lower row) Masaru Kito, Tomoharu Matsushita**, Hideaki Aochi*, Hiroyasu Tanaka*, Akihiro Nitayama*, Ryota Katsumata* and (Upper row) Masaru Kido*; *Inventor, ** Chief Production Executive of KIOXIA Corporation (by permission of KIOXIA)*

to the substrate and stabilize the variability of the contact resistance.

The first results of an experimental 512 kbit test chip were presented at the 2007 VLSI Symposium [19]. The team was successful in presenting the results of functional 32 Gbit density memory arrays, obtained in 2008, at the 2009 VLSI Technology Symposium [21].

Aochi underlines: "*That announcement impacted all of flash memory manufacturing and accelerated similar type of flash memory development. We had made the first production chip of 48-layers of BiCS FLASH™ with 256 Gbit memory density in 2015.*" Obtaining reproducible hole shape strings was a major critical path.

Toshiba announced at ISSCC 2019 a 1.33 Tbit chip based on the 3D BiCS FLASH™ technology stacking 96 layers and 4 bit/cell [22].

After the successful implementation of the BiCS-FLASH™ technology by Toshiba and continued by Kioxia, 3D vertical Flash memories have become very popular for mass storage among the main memory makers. After producing stacked 2D structures [18], Samsung followed an approach close to Toshiba's and demonstrated a vertical 3D structure integrating a damascene p+-like W gate, ancestor of a vertical TaNOS structure [23].

Nowadays, 3D Terabit class memory can be integrated in a single chip, stacking up to 128 layers, featuring up to 4 bits/cell and a bit surface density approaching 10 Gbit/mm^2. The memory circuits can be handheld in a solid state disk or equip mass storage systems in data centers. The 3D string-type Flash Memories have been adopted among Toshiba/KIOXIA competitors as well, either with a SONOS/p+-like TaNOS or vertical Floating gate structures [23]–[26].

Many other candidates featuring alternative structures or materials have been trying to take over their success. These are floating gate-inspired (i.e. Si Nanocrystal FG, split gate, NROM structures, etc.) or based on 1 to 2 transistors associated to a resistor or capacitor(s) (i.e. MRAMs, STT RAMs, ReRAMs, FeRAMs, etc.) to reduce the SILC issue or address a storage node. Their compatibility or co-integration with Si CMOS is sometimes a strong requirement. Some of these alternative solutions could be or have already been adopted as application specific, field programmable gate arrays (FPGAs), embedded memories or distributed in CMOS for new computing paradigms and ultra low power circuit architectures (i.e. neuromorphic computing and programmable circuits, non-volatile logic and RAMs, etc.) [27]. These latter topics have not been addressed in this issue, due to the vast extent of the subject, as they would request another article.

The discovery of the Floating Gate and discrete trapping concepts augmented by the invention of Flash Memories are with no doubt major events in the history of microelectronics and its success. They have sustainably impacted our daily life with broad societal usage. Their most recent success for 3D mass storage was possible thanks to a succession of microelectronics engineering marvels developments.

Acknowledgements to Prof. Simon Sze (NCTU), Prof. Fujio Masuoka (Tohoku University), Dr. Koji Sakui (Honda), Prof. Masaaki Inutake (Tohoku University), Drs. Hiroyasu Tanaka, Ryota Katsumata, Hideaki Aochi, and Kazunari Ishimaru (KIOXIA).

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IMPORTANT: THE CONFERENCE NOTICES IN OUR SOCIETY NEWSLETTER WERE PUBLISHED BEFORE THE ESCALATION OF THE COVID-19 PANDEMIC. MANY IEEE CONFERENCES ARE ALTERING THEIR ARRANGEMENTS. PLEASE CONSULT EACH CONFERENCE WEBSITE FOR THE MOST UP-TO-DATE INFORMATION.

Upcoming Technical Meetings

2020 IEEE Photovoltaics Specialist Conference (PVSC)

By Seth Hubbard and Geoffrey Bradshaw

It is our great pleasure to invite you to attend the 47th IEEE Photovoltaics Specialists Conference, which will be held from June 14–19, 2020, at the Telus Convention Center in Calgary, Alberta, Canada.

We live at a special time when solar electricity has become cost competitive with conventional electricity in many locations, enabling remarkable growth of the industry. As was the case in 2017, solar was the biggest contributor to net expansion of electricity generating capacity in 2018. In fact, the IEA PVPS has recently reported that worldwide solar installed capacity has now crossed the half TW mark! The 47th IEEE PVSC will help sustain this fantastic momentum with over 800 technical papers from around the world, reflecting today's dynamic and expanding markets. The PVSCs have a rich tradition of bringing together students, innovators, researchers and PV leaders in a vibrant and highly integrative forum to share information, gain knowledge, strengthen collaborations and move forward photovoltaic science and technology from basic and applied research into large scale manufacturing and deployments.

If you would still like to contribute technically, please submit your abstract before our late news deadline on April 20, 2020.

Continuing with the tradition of the past few years, the 47th IEEE PVSC will be divided into 12 technical areas covering cutting-edge developments in science and engineering of photovoltaics, ranging from fundamentals to applications, with an emphasis on material science, devices, systems, solar resources and policy related matters. PVSC-47 aims to be a highly interactive venue for both seasoned PV experts as well as entry-level professionals and students. The conference provides a unique opportunity to meet, share and discuss PV-related developments in a timely and influential forum. Please consider contributing to the PVSC's tradition as the premier international conference on PV science and technology and help us propel the world towards power from the Sun. As well, we will be presenting the prestigious William R. Cherry Award, honoring the photovoltaics communities' most outstanding scientist or engineer as well as the Stuart R. Wenham Young Professional Award for individuals who have made significant contribution at an early stage of their career.

Calgary, Canada skyline

The conference Exhibition will showcase the latest developments in PV characterization and manufacturing equipment, and is set to further enhance attendee awareness on latest tools and instrumentation as well as to facilitate exchange between scientists, technical experts and exhibitors.

We are very excited to host the first ever PVSC to be held in Canada. Calgary is a beautiful city in the heart of Canada situated on the eastern slope of the magnificent Canadian Rockies mountain range. As the fourth-largest and the sunniest city in Canada, Calgary has a lot to offer visitors from around the world. Calgary has one of the highest concentrations of green space in North America, and is the first municipality in Canada to power its infrastructure solely by renewable energy.

(continued on page 13)

Register Now for the IEEE IITC 2020 Conference

IITC 2020 will be held June 1-4, 2020 in the heart of Silicon Valley at the newly renovated campus of the Holiday Inn San Jose—Silicon Valley, easily accessible from San Jose International Airport. One of the highlights will be a special evening event at The Tech Interactive in downtown San Jose.

IITC is the premier conference for interconnect technology and will offer leading-edge research in the field of advanced metallization and 3D integration for ULSI IC applications. The conference will highlight innovative research and development in the critically important field of on-chip interconnects, integration and metallization, including design, unit process, integration and reliability.

The conference will kick off with a one-day workshop on June 1st:

Model Your Way to a Better Backend Technology Workshop Program

In this workshop, leading scientists and innovators will review the modeling approaches used in industry and academia, providing a powerful

means to predict the performance of continuous scaling and integration of new interconnects and memories on chip. They will also show benchmarking of various materials and device technologies.

We are excited to have the following Keynote Speakers:

- **Dr. H.-S. Philip Wong**, VP of Corporate Research at TSMC and the William R. and Inez Kerr Bett Professor at Stanford University.
- **Dr Michael Mayberry**, Chief Technology Officer and Senior VP and GM of Technology Development at Intel.

Our Invited Speakers include:

- Jeong-Hoon Ahn, Samsung
- Kristof Croes, imec
- Suman Datta, University of Notre Dame
- Regina Freed, Applied Materials
- Arnaud Furnemont, imec
- Oleg Gluschenkov, IBM
- Chris H. Kim, University of Minnesota
- Eiich Kondoh, University of Yamanashi
- Nick Lanzillo, IBM
- Takeshi Nogami , IBM
- Jon Reid, Lam Research
- Harsono Simka, Samsung
- Shintaro Yamamichi, IBM Japan

Presentation topics for invited speakers may be found on at https://iitc-conference.org/invited-speakers/

Full conference and workshop details may be found at https://iitc-conference.org

IITC 2020 is sponsored by the IEEE Electron Devices Society.

Registration:

Conference registration is now open at https://iitc-conference.org/registration/

Early Registration deadline: May 8, 2020

IITC-2020 Conference Co-Chairs:

Paul Besser, Robert Socha and Soo-Hyun Kim

The 2020 Symposium on VLSI Technology Looks Ahead to "The Next 40 Years of VLSI for Ubiquitous Intelligence" in Honolulu, Hawaii

The premier international conference on **VLSI semiconductor technology** is celebrating its 40th year of delivering unique perspectives on the convergence of VLSI technology in the microelectronics industry. The 2020 Symposia on VLSI Technology & Circuits is organized on the theme: "The Next 40 Years of VLSI for Ubiquitous Intelligence," and will be held from June **14th to 19th, 2020**, at the Hilton Hawaiian Village in Honolulu, Hawaii, USA. The symposia are jointly sponsored by the IEEE Electron Device Society (EDS) in cooperation with the IEEE Solid-State Circuits Society (SSCS) and the Japan Society of Applied Physics.

Held jointly on a fully-overlapping schedule from June 14th to 19th, 2020 in Hawaii with the Symposium on VLSI Circuits, the two Symposia integrate advanced technology developments, innovative circuit design, and the applications they enable, such as machine learning, IoT, artificial intelligence, wearable/implantable biomedical applications, big data, cloud/edge computing, virtual reality (VR)/augmented reality (AR), robotics, and autonomous vehicles. As such, the combined Symposia provide a unique perspective that promotes interactions between technologists and circuit/system designers, reflecting the close relationship between R&D in both areas required to achieve continuous improvement in performance, power efficiency, connectivity, and cost reduction. This integration between innovations in devices and circuits helps foster new technologies, processes, and applications. A single registration fee covers both events.

As part of this integration, this year the Symposia will once again feature special joint focus sessions to provide opportunities for both Technology and Circuits attendees to exchange ideas on areas of joint interest that enable ubiquitous intelligence, smart mobility, and other VLSI applications, including: "MRAM Future: Beyond STT, Beyond Embedded," "Silicon Photonics," "5G/mm-wave," "System/Design-Technology Co-Optimization," "Artificial Intelligence/Machine Learning," and "Heterogeneous Integration."

Rainbow Tower, Hilton Hawaiian Village, Honolulu, Hawaii - a venue of the 2020 VLSI Symposia

Once again, the Symposia will be followed by a full-day Friday Forum session dedicated to "Technologies & Circuits for Edge Intelligence," led by experts in the field who will help guide participants in discussions on the contributions of technology and circuits needed to drive the future of advanced edge computing.

Additional highlights include:
Plenary sessions for both Technology and Circuits with four talks:

- Dr. Michael C. Mayberry, chief technology officer at Intel Corporation, "The Future of Compute: How the Data Transformation is Reshaping VLSI,"
- Takehiro Nakamura, senior vice president & general manager of 5G Laboratories, NTT DOCOMO, "5G Evolution and 6G,"
- Shigeo (Jeff) Ohshima, technology executive at KIOXIA (formerly Toshiba Memory), "Empowering Next-Generation Applications through FLASH Innovation"
- Jen Lloyd, vice president for the Precision Technology & Platforms Group, Analog Devices, "Performance that Matters at the Real World Interface."

Three Evening Panel Discussions:

- "40 Years of VLSI to Enable the Future of Computing"
- "Memory & Logic Technology Divergence: Will AI/ML Bring Them Back Together?
- "Human vs. Machine: The Future Role of AI/Machine Learning in Circuit Design"

Full-day short courses. Attendees will learn about recent trends and challenges in advanced microelectronics

technology and its adaptation into new computing systems:

- "Future of Scaling for Logic & Memory
- "System, Technology, & Design Solutions for Heterogeneous Integration"
- "Trends & Advancements in Circuit Design"

Sunday Workshops. (Held June 14th before the technical sessions):

- "Know Where You Are Going: Metrology in the New Age of Semiconductor Manufacturing"
- "Analog Computing Technologies & Circuits for Efficient Machine Learning Hardware"
- "Quantum Computing: Maximizing the Impact of the Semiconductor Industry"

Satellite workshops (held before the technical session of the symposium):

- "IEEE Silicon Nanoelectronics Workshop" (June 14th & 15th)
- "Spintronics Workshop on LSI" (June 14th) at the same location.

We cordially invite you to attend the 2020 Symposium on VLSI Technology. For further information please visit the VLSI Symposia website: www.vlsisymposium.org.

Technology Symposium Chairman:
Chorng-Ping Chang (USA)
Applied Materials

Technology Symposium Co-Chairman:
Yamakawa Shinya (Japan)
Sony Semiconductor Solutions

Technology Program Chairman:
Tomas Palacios (USA)
Massachusetts Institute of Technology

Technology Program Co-Chairman:
Katsura Miyashita (Japan)
Toshiba Electronic Devices & Storage

2020 IEEE Photovoltaics Specialist Conference (PVSC)

(continued from page 10)

Don't miss out on the opportunities offered by the conference social gatherings and networking events to get to know your colleagues better, reconnect with old friends and make new ones. The week kicks off with our Exhibitor Reception on Monday evening at the Convention Center and will conclude with a Conference Reception on Thursday evening to be held at Calgary's Glenbow Museum, with exhibits and performances that bring the art and culture of Calgary to life.

On behalf of the Organizing, Cherry, and International Committees, we look forward to welcoming you to the 47th PVSC in Calgary, Canada!

Further details and registration can be found at https://www.ieee-pvsc.org/PVSC47/

Seth Hubbard
Conference General Chair
Rochester Institute of Technology

Geoffrey Bradshaw
Conference Publicity Chair
Pike Engineering, LLC

Dear EDS Newsletter Readers,

Due to the global pandemic, many conferences are altering their arrangements. Due to this fact, we did not publish the Technical Meeting Calendar in this issue. We are very sorry for this. Please consult each conference website for the most up-to date information. We do hope that people and organizations involved in a campaign against the SARS-CoV-2 worldwide will succeed in the near future. We wish all the best to you and to your beloved.

EDS Newsletter Editorial Team

Society News

A message from Editor-in-Chief

Dear EDS Members and Readers,

Daniel Tomaszewski Editor-in Chief, EDS Newsletter

The IEEE Electron Devices Society (EDS) is a world-wide community of experienced researchers and engineers, young professionals, and students working in the area of electron device (ED) technology. Our community needs a platform for sharing news about global and local initiatives and undertakings in this field and for sharing information on the Society growth with emphasis on the EDS chapter activities, taking into account their professional and societal aspects. EDS Newsletter serves as such a platform for the benefit of the EDS healthy and sustainable growth.

I have been involved in the EDS Newsletter activity since 2015. Then Dr. Wladek Grabinski recommended me for a position of EDS Newsletter Regional Editor for Region 8 Eastern Europe. After a positive evaluation of my candidacy by the Newsletter Oversight Committee, Dr. M.K. Radhakrishnan, Editor-in-Chief invited me to join the Editorial Board. Since then, I have constantly experienced a very kind support and leadership from M.K.R. and next, from Dr. Carmen Lilley as Editors-in-Chief, as well as a kind assistance from Joyce Lombardini coordinating a work of the Editorial Board. I am deeply grateful to them for the collaboration and guidance. In October 2019 I was asked, surprisingly for me, whether I agreed to candidate for the Editor-in-Chief position. I agreed … and was approved for a three-year term. Here I have to express my gratitude and thanks to colleagues from EDS Chapters in Georgia, Macedonia, Ukraine, Romania, Russia with whom I was collaborating since 2015. They do have a significant contribution to this nomination.

So, a new challenge for me with an incomparably larger scope of responsibilities has appeared. I am aware, that I will be able to fulfill my duties and meet the requirements only if I follow the rules and procedures, and closely collaborate with the Editorial team. In order to implement the mission indicated above I am going to continue the work of M.K.R. and Carmen. I also hope that they will share their experience with me, if I ask them for help, in particular if plans to enhance the Newsletter appear. This Issue of the Newsletter has been edited jointly by Carmen and myself with an invaluable support by Joyce.

I am looking forward to working with the EDS Officials, who provide messages to the Society through the Newsletter, with the EDS Technical Committees and with the EDS Staff, providing the Newsletter issues with a lot of technical information on the Society daily activities. I am looking forward to collaborating with the Regional Editors who publicize various activities, news, and highlights of Young Professionals, EDS chapters and members. I am also looking forward to communicating with organizers of the technical meetings and conferences, to publicize in advance and report these events for the benefit of EDS members and Newsletter readers. I also would like to maintain, and enhance, if possible, information on EDS Distinguished Lectures, DL Mini-Colloquia, webinars, i.e. platforms helpful for publicizing ED technology issues among the Newsletter readers.

As well, following the first message from Carmen as the EiC, I would like to invite the EDS members and readers to share with the Editorial Board their ideas on themes they would like to appear in the Newsletter and feedback on changes you see in the Newsletter in the coming years.

Finally, let me share a message with you, that a new member is joining the Editorial team. Dr. Kateryna Arkhypova from O.Ya. Usikov Institute for Radiophysics and Electronics of the National Academy of Sciences of Ukraine (IRE NASU) has been appointed as the Regional Editor for Region 8 Eastern Europe. It is my pleasure to welcome her in our team. Dear Kateryna, I wish you a fruitful work for the EDS community.

Kateryna Arkhypova

Kateryna Arkhypova (M'15-SM'19) received the M.S. and Ph.D. degrees in Biophysics from V.N. Karazin Kharkiv National University, Ukraine, in 2006 and 2012, respectively. Since 2005 she has been with O.Ya. Usikov Institute for Radiophysics and Electronics, NAS of Ukraine, where she is now a Senior Researcher. Her research interests are oriented towards clinical applications of microwaves for diagnostic and therapeutic purposes. Dr. Arkhypova has more than 10 years of experience in multidisciplinary scientific cooperation with life scientists (primarily, medical doctors, biologists, and biochemists). She is an active IEEE volunteer. She is a Chairperson of the IEEE Ukraine Section (East) AP/MTT/ED/AES/GRS/NPS Societies Joint Chapter as well as a TPC member of various international conferences such

as European Microwave Conference, IEEE MTT-S International Microwave Bio-Conference, IEEE Ukrainian Microwave Week, etc. Since 2019, she also serves as the EuMA General Assembly member representing Group 10 (Armenia, Azerbaijan, Georgia, Moldova, and Ukraine).

Sincerely,
Daniel Tomaszewski
Editor-in Chief, EDS Newsletter
e-mail: dtomasz@ite.waw.pl

Message from EDS Vice President for Regions and Chapters

Murty Polavarapu
EDS Vice President of Regions and Chapter

It is my privilege to serve the members of EDS as Vice President for Regions and Chapters for 2020–2021. It is particularly gratifying for me since my first IEEE volunteer role was as the EDS Chapter Chair in the Washington, DC area.

Chapters are geographical units of our Society and provide resources to members at local level for professional networking and learning. At Chapter meetings, you can develop and nurture professional relationships with your peers in the local area and get to meet leading authorities in your field who volunteer their time to share their knowledge of latest developments in an informal setting. As a volunteer at Chapter level, you can further develop your IEEE network and be able to assume roles with increasing responsibility in the world's largest professional society.

There are over 200 EDS Chapters worldwide and chances are that there is an EDS Chapter in your geographical area. You can find your local chapter at https://eds.ieee.org/chapters/global-chapters-list. The EDS provides significant resources to Chapters in the form of funding for Distinguished Lecturers, Mini-colloquia and Chapter subsidies. In addition, the best performing Chapters are recognized annually with awards. More information on these resources is available on the EDS website https://eds.ieee.org/.

Each IEEE Chapter is connected to a local geographic Section. As such, a Chapter has two parents—Section and Society. Financial support for active Chapters (also known as annual rebate) is available through Sections from IEEE Member and Geographic Activities (MGA). Sections are also expected to provide support to Chapters in financial management and communications to all local members (beyond the EDS members). The vTools platform provided by MGA is a valuable resource to all local units in organizing meetings and in reaching the target audience electronically. For more information visit https://site.ieee.org/vtools/.

EDS also has many Student Branch Chapters based at educational institutions. With the normal expectation of student turnover, these units face severe challenges in organizing activities and maintaining membership. The faculty advisors can play an important role here in mentoring students and in instilling in them the value of belonging to a professional society.

Lack of new volunteers is frequently cited as the main reason for many chapters being inactive. Volunteer recruitment is not easy if you are trying to get someone to make a commitment to fill a role at the Chapter level for a full year. You may want to ease a potential volunteer into Chapter activities by asking for help with a small task, for example, for finding a venue for the next Chapter meeting. This is called 'microvolunteering' and if you can get ten people to help with small tasks, at least one of them most probably will volunteer for the longer term. Give it a try!

From the governance perspective at the Society level, these geographic activities come under the purview of Regions/Chapters Committee and at a Regional level by the Subcommittees for Regions and Chapters (SRCs). I am deeply thankful for all the senior volunteers who have accepted the responsibilities on these Committees. The SRCs are expected to play an active role in nurturing Chapters in their geographical areas and provide resources as needed. SRCs are also called upon to help assess the viability of new chapters and mentor weak chapters. I hope to leverage the knowledge and networks of the members of the Regions/Chapters Committee and the SRCs in re-energizing our Chapters.

I urge you to seek out your local chapter and get involved as a volunteer or at least offer to share the results of your work at a meeting. You will find it a rewarding experience!

Murty Polavarapu
EDS Vice President of Regions and Chapter
Space Electronics Solutions

More information available at https://eds.ieee.org/about-eds/governance/standing-committees/regions-chapters-committee

Subcommittee Roster for Regions and Chapters available at https://eds.ieee.org/about-eds/governance/standing-committees/subcommittee-for-regions-chapters

Announcement of Newly Elected Officers & BoG Members

The Electron Devices Society (EDS) Officers and Board of Governors (BoG) members-at-large election was held on December 8, 2019 in San Francisco, CA. I am pleased to present the results of this election and short biographical information of the incoming team that will lead EDS in the years to come.

OFFICERS

The following volunteers were elected as Officers beginning 1/1/2020:

President-Elect

Ravi Todi received his doctoral degree in electrical engineering from the University of Central Florida (UCF), Orlando, Florida. In his early career as an advisory engineer/scientist at the semiconductor research and development center at IBM microelectronics, his work was focused on high performance eDRAM integration on 45-nm silicon-on-insulator logic platform. For his many contributions to the success of eDRAM program at IBM, Ravi was awarded IBM's prestigious outstanding technical achievement award. In 2012, Ravi Joined Qualcomm for 20-nm product development and foundry management group, responsible for Qualcomm's foundry engagement with leading foundries. In 2015, he joined GLOBALFOUNDRIES, as the director of 14-nm product-line management, where he and his team were responsible for driving the technical and business results of the 14-nm FinFET product offerings. Currently he is with the Western Digital as a Sr. Technologist responsible for foundry technology development for global ASICs. With over 60 US granted patents, over 30 peer-reviewed journal publications, over 40 international conference presentations, and over 50 invited distinguished lectures, Ravi is well known in the semiconductor industry as a technical/business leader. He is a Fellow of the IEEE, a distinguish lecturer of IEEE EDS and serves as an editor of the IEEE Transactions on Electron Devices. He has served as an IEEE EDS Treasurer for four years, an elected BOG member, and as the Vice President of Technical Activities and conferences. Currently, he is the President-Elect of IEEE EDS.

Treasurer

Bin Zhao received his Ph.D. degree from California Institute of Technology. He has been with SEMATECH, Rockwell, Conexant, Skyworks, Freescale, Fairchild, ON Semiconductor, and has worked on advanced VLSI technology development and design implementation of analog/mixed-signal, power management, and RF IC products. He has authored and coauthored over 200 journal publications and conference presentations, has authored three book chapters, and holds over 70 issued US patents. He has served as the Founding Co-Chair, Technical Working Group of RF and Analog/Mixed-Signal IC Technologies for Wireless Communications, International Technology Roadmap for Semiconductors (ITRS); IEEE EDS VP of Conferences; IEEE EDS VP of Publications; Chair, Editorial Steering Committee, IEEE Journal of Microelectromechanical Systems (J-MEMS); and Chair, IEEE Johnson Technology Award Committee. He is an IEEE Fellow and currently serving as the Chair of IEEE Conference Committee. He is a member of the IEEE Technical Activities Board, IEEE Publications Services and Products Board, and IEEE IoT Activities Board.

Secretary

MK Radhakrishnan is an academician and technical consultant in the field of electron device failure analysis and reliability, and founder director of NanoRel LLP Technical consultants Singapore from 2004. Previously, he was a Senior Member of the Technical Staff at the Institute of Microelectronics, Singapore, an Adjunct Professor at the National University of Singapore, and a Scientist at the Indian Space Research Organization. Currently he is an Editor of the IEEE Journal of Electron Devices Society (JEDS). He has served as Editor of the Journal of Semiconductor Technology and Science and Guest Editor to IEEE TDMR. He was the Technical Chair of the IEEE IPFA in 1995 and 1997, General Chair of IPFA 1999 and IEEE IEDST 2009, and Co General Chair of IEEE EDTM 2019. As an IEEE EDS volunteer he served as an IEEE EDS Region 10 SRC Vice Chair, Regional Editor and the Editor in Chief of the EDS Newsletter, a member of the IEEE EDS Board of Governors, and IEEE EDS Vice President of the Regions & Chapters. He is an IEEE Life Senior member, Fellow of IETE, Member of the EDFAS and ESDA, and serves as an IEEE EDS Distinguished Lecturer.

BoG Members-At-Large

A total of seven members were elected for a three-year term (2019–2021). Two of the seven electees are serving a second term, while the other five have joined the board for the first time. The backgrounds of the electees span a wide range of professional and technical interests. The following are the results of the election and brief biographies of the individuals elected.

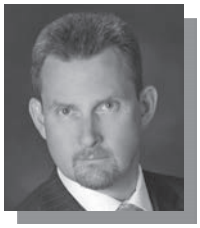
Constantin Bulucea received his MS (1962) and PhD (1974) degrees in EE

from the Polytechnic Institute of Bucharest. In 1969, he won a one-year scholarship for graduate studies at UC Berkeley.

Between 1970 and 1986, he led the R&D activities of Romania's Research Institute for Electronic Components, ICCE. In 1978, following the model of IEDM, he founded the Annual Conference for Semiconductors, now an international IEEE event. In the US, Dr. Bulucea worked for Siliconix, National Semiconductor, and TI (1987-2012) developing the first trench DMOS power transistors of the industry (Siliconix), and several high-performance analog CMOS processes (National Semiconductor). His inventions are protected in 69 US patents. Dr. Bulucea has been an editor of SSE (1978-2012), IEEE EDL (1995-2012), and IEEE J-EDS (2013 -). He is an Honorary Member of the Romanian Academy and an IEEE Life Fellow. In 2018 and 2019 he was on the IEEE/EDS Fellow Evaluation Committee.

Daniel Camacho M.Sc. Received his BSEE from the Pontificia Universidad Javeriana in Bogota, Colombia in September 2007. He was awarded the 2008 IEEE EDS Master Student Fellowship for his research work. In 2009 he received his Master's degree from Southern Methodist University in Dallas, Texas. He joined the Intel Corporation in 2010, where he has been since. His expertise is focused on high-performance analog and mixed-signal circuits, and clock generation and distribution.

John Dallesasse is a Professor of Electrical and Computer Engineering at the University of Illinois at Urbana-Champaign and has over 20 years of industry experience in technology development and executive management. Prior to joining UIUC he was



the Chief Technology Officer, Vice President, and co-founder of Skorpios Technologies developing innovative methods for heterogeneous integration of compound semiconductors with silicon. His technical contributions include, with Nick Holonyak, Jr., the discovery of III V Oxidation, which has become an enabling process technology for the fabrication of Vertical-Cavity Surface-Emitting Lasers (VCSELs) for optical networking, 3D imaging, and LIDAR applications. John has a strong publication history and 45 issued patents. He serves as the Secretary of the Steering Committee for the IEEE Journal of Lightwave Technology and is the Chair of the Steering Committee for the IEEE Transactions on Semiconductor Manufacturing. He is a Fellow of the IEEE and OSA.

Mario Lanza received his PhD (with honors) in Electronic Engineering in 2010 at the Universitat Autonoma de Barcelona. In 2010–2011 he was NSFC postdoc at Peking University, and in 2012–2013 he was a Marie Curie fellow at Stanford University. Currently, he is a Full Professor in Nanoelectronics as Soochow University, where he leads a group formed by 17-20 graduate students and postdocs. His research focuses on the improvement of electronic devices using 2D materials. Prof. Lanza has published over 120 research papers (including Science, Nature Electronics, IEDM) edited a book for Wiley-VCH, and registered four patents, one of them granted with 1 million USD investments. He is member of the technical committee of several conferences (IEDM, IRPS, IPFA) and journals (Advanced Electronic Materials, Nature Scientific Reports, Nanotechnology). Prof. Lanza has received several world-class awards in his field of research, and he is a Distinguished Lecturer of the Electron Devices Society.

Geok Ing Ng received his Ph.D degree from the University of Michigan, Ann Arbor in 1990. Since joining the Nanyang Technological University (NTU) Singapore in the School of EEE in 1996, he has held several key appointments including the Head of Microelectronics Division and Founding Directors of Microsystem Technologies Development Centre. He is currently the Director of the Center for Microsystems in TL@NTU and the Centre of Micro- and Nano-Electronics in EEE. He has published more than 300 international journal and conference papers and delivered plenary and invited talks at several international conferences in the areas of III-V low bandgap (InP) and large bandgap (GaN) compound semiconductors. He has been active in serving IEEE in various capacities including Steering Committee Member, 2020 IEEE Electron Device Technology and Manufacturing (EDTM) Conference, General Co-Chair, 2019 IEEE EDTM Conference, Guest Editor of Special Section of IEEE Transactions on Nanotechnology.

Claudio Paoloni received the degree cum laude in Electronic Engineering from the University of Rome "Sapienza", Italy, in 1984. Since 2012, he has been Cockcroft Chair with the Engineering Department, Lancaster University, U.K. Since 2015, he has been the Head of Engineering Department. He is IEEE Senior member and Senior Fellow of the Higher Education Academy. He is Chair of the IEEE Electron Devices Society Vacuum Electronics Technical Committee (2017–present). He was a Guest Editor for the Special

Issue of the Transactions on Electron Devices on Vacuum Electronics (June 2014). He organized numerous international conferences and workshops, on vacuum electronics, millimetre wave and terahertz communications and technology. He is coordinator of two European Commission Horizon 2020 projects, TWEETHER and ULTRAWAVE. He is the author of more than 230 articles in international journals and conferences in the field of high frequency electronics, millimetre waves and THz vacuum electronics devices, and wireless communications.

Hitoshi Wakabayashi (M'00) received the M.E. and Ph.D. degrees in electrical engineering from the Tokyo Institute of Technology, Japan, in 1993 and 2003, respectively. He was with NEC Corporation from 1993 to 2006, the Massachusetts Institute of Technology from 2000 to 2001, and Sony Corporation from 2006 to 2012. He has been with the Tokyo Institute of Technology since 2013. He has served as the General Chairs for the Symposium on VLSI Technology 2013, EDTM 2018, and IWJT 2017/2019.

I welcome all electees and urge them to get fully engaged in the affairs of the Electron Devices Society. EDS is a volunteer-led volunteer-driven organization and we expect the incoming volunteer leaders will continue this tradition going forward.

Samar Saha
2019 EDS Nominations and Elections Chair
Prospicient Devices
Milpitas, CA

In Memory of Harvey C. Nathanson

by Joachim N. Burghartz

On Friday, November 22, 2019, at age 83, Harvey C. Nathanson peacefully passed away at home while with his loving family. Shortly prior to that date I happened to finish the article "Marvels in MEMS Evolvement and Development—Silicon as a Micromechanical Material has been Driving More-than-Moore" which recently appeared in the EDS Newsletter of January 2020 as part of the series "Marvels of Microelectronic Engineering". Harvey Nathanson played the most significant role in that article in which the key achievements and developments as well as the people behind MEMS were highlighted. Harvey Nathanson was the father of the MEMS. His work can be considered the first step into surface micromachining, in which the planar wafer processes were exploited for shallow three-dimensional micromechanical structures above of the bulk silicon wafer. What he started in the 1960's has become the foundation of MEMS devices which today can be found in virtually any commercial and consumer application. Reaching the high age of 83, Harvey Nathanson could enjoy seeing the blossom of his work.

Esther Mishelevich Nathanson, his wife, told me about his life and career,

which already was highlighted in an obituary in the Pittsburgh Gezette on November 23/24, 2019: He grew up in Pittsburgh as the son of a pharmacist and remained to stay there for all his life. As a boy in the 1950s, he taught himself about electrical circuits and built hi-fi music systems from mail-order kits. Instead of stepping into the footsteps of his father and take over the family pharmacy business he went to Carnegie Tech, now Carnegie Mellon University, where he earned his MS and Ph.D. degrees, both in electrical engineering. He joined Westinghouse Electric in Pittsburgh, working at Westinghouse Research Labs in Churchill. In 1965 he thought of a microscopic device used as a tuner for microelectronic radios. The invention, known as the resonant-gate transistor, became the first device in the field of micro-electro-mechanical systems (MEMS). This technology is now found in consumer products ranging from iPhones to automobiles. Harvey Nathanson also pioneered a method of mass production that would later become a mainstay of MEMS manufacturing. In 1973, he patented the use of tiny mirrors to create a video display of the type now found in digital projectors. In 1988 he became Chief Scientist of Westinghouse Research Labs, from where he retired in 2001 but continued to consult for another decade, completing a 50-year career in which he was awarded more than 50 patents in the field of solid-state electronics. In 2000 Nathanson was awarded the Millennium Medal by the Institute of Electrical and Electronics Engineers for "outstanding contributions to the Society and to the field of electron devices".

Harvey Nathanson is one of the great pioneers in the broader field of electron devices. We consider it an honor to further build on his ideas.

Meyya Meyyappan wins Technology Champion Award for Flexible Electronics

SEMI-FlexTech gives the FLEXI Awards each year to the winners for outstanding achievements in Flexible Hybrid Electronics (FHE). Meyya Meyyappan, current EDS President, received the 2020 Technology Champion FLEXI Award for "his technical leadership in printed and flexible electronics, outreach activities and tireless volunteering to promote the field" at the FLEX 2020 Conference in San Jose, California, on February 26, 2020. FLEXIs have been the industry's premier award for distinguished organizations and individuals in the FHE sector since 2009. The awards are sponsored by SEMI-Flex Tech, an organization dedicated to the success of the FHE sector.

2020 IEEE EDS Robert Bosch Micro and Nano Electro Mechanical Systems Award Winner

The 2020 IEEE EDS Robert Bosch Micro and Nano Electro Mechanical Systems Award was presented to Ming C. Wu, University of California, Berkeley, CA, USA, at the 2020 IEEE MEMS Conference, Vancouver, Canada, January, 2020. This prestigious award recognizes and honors advances in the invention, design, and/or fabrication of micro- or nano-electromechanical systems and/or devices.

Ming C. Wu is the Nortel Distinguished Professor of Electrical Engineering and Computer Sciences at University of California, Berkeley, and Co-Director of Berkeley Sensor and Actuator Center (BSAC). He received his PhD from UC Berkeley in 1988 and joined its faculty in 2004 after working at AT&T Bell Laboratories and UCLA. He has published 600 papers and holds 30 US patents in Optical MEMS, optofluidics, silicon photonics and optoelectronics. In 1997, Prof. Wu co-founded OMM to commercialize MEMS optical switches. Recently, his group extended the switch array size to 240 x 240 by combining MEMS with silicon photonics. In 2011, Prof. Wu co-founded Berkeley Lights, Inc. to commercialize optoelectronic tweezers (OET) for single cell biology applications. Prof. Wu is an IEEE and Optical Society Fellow. His work has been recognized by the 2007 Paul F. Forman Engineering Excellence Award (OSA), the 2016 William Streifer Scientific Achievement Award (IEEE), and the 2017 C.E.K. Mees Medal (OSA).

Ming C. Wu
For pioneering contributions in MEMS optical switches and optoelectronic tweezers

Kurt Petersen
EDS Bosch Award Chair

IEEE ROBERT BOSCH
MICRO AND NANO ELECTRO MECHANICAL SYSTEMS AWARD

Robert Bosch (1861-1942)
Inventor, Entrepreneur, Founder of Robert Bosch GmbH

The Robert Bosch Micro and Nano Electro Mechanical Systems Award was established by the IEEE Electron Devices Society in 2014, to recognize and honor advances in the invention, design, and/or fabrication of micro- or nano-electromechanical systems and/or devices. The contributions to be honored by this award should be innovative and useful for practical applications.

This award is sponsored by the IEEE Electron Devices Society, with financial support from Robert Bosch LLC. It is intended that the award will be presented annually to an individual or to as many as three individuals whose achievements and contributions are judged to meet the selection criteria for the award. The award will be presented at an IEEE conference of the winner's choice. It is not necessary for the recipient(s) to be a member(s) of IEEE.

The recipient will receive a US$10,000 honorarium, travel expenses to attend the award presentation, a bronze medal, and a certificate. In the event that more than one awardee is selected the cash honorarium will be equally divided among the recipients. Each recipient will receive a bronze medal and a certificate.

Please visit the EDS website for more information on this award: http://eds.ieee.org/robert-bosch-micro-and-nano-electro-mechanical-systems-award.html.

Nominations for this award should be made using our online nomination form, and submitted before midnight (EST) on October 2nd. Letters of recommendation must be sent directly to l.riello@ieee.org according to the same schedule.

2019 IEEE EDS Distinguished Service Award

The IEEE Electron Devices Society (EDS) is extremely proud of the services that it provides to its members. Its members generate the premier new developments in the field of electron devices and share these results with their peers and the world-at-large by publishing their papers in EDS journals and presenting results in its meetings. This is a global activity that is effective because of the efforts of numerous volunteers. Many of these volunteers labor in relative obscurity, with their only reward being the satisfaction that they receive in being an important part of a successful organization, namely of the IEEE Electron Devices Society. One means of thanking these volunteers is to recognize their contributions through the EDS Distinguished Service Award.

The recipient of the 2019 EDS Distinguished Service Award was Albert Wang, University of California, Riverside, CA, USA, and the award presentation took place at the International

Albert Wang, 2019 IEEE EDS Distinguished Service Award winner and Fernando Guarin, 2019 IEEE EDS President

Electron Devices Meeting (IEDM) in San Francisco, CA on December 9, 2019.

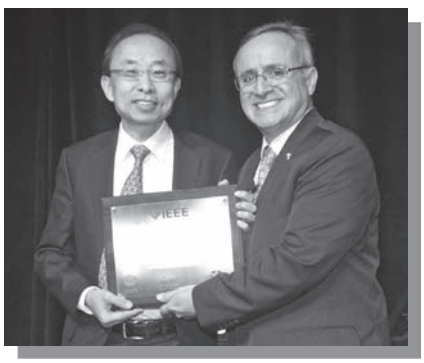
Albert Wang received BSEE from Tsinghua University, China, and PhD EE from State University of New York at Buffalo, USA. He was with National Semiconductor Corporation before joining the Faculty of Illinois Institute ofTechnology. He is a Professor of ECE at University of California, Riverside, USA. His research covers RF/AMS ICs, Integrated Design-for-Reliability, 3D Heterogeneous Integration, Emerging Nano Devices and Circuits, and LED-based Visible Light Communications. Wang received NSF CAREER Award. He published one book and 260+ papers, and holds 16 US patents. He was editor for IEEE EDL, TED, TCAS I&II, and JSSC. Wang was IEEE Distinguished Lecturer for IEEE Electron Devices Society, IEEE Solid-State Circuits Society and IEEE Circuits and Systems Society. Wang was Sr. Past President (2018–2019), and was Jr. Past President (2016–2017) and President (2014–2015) of IEEE Electron Devices Society. Wang is IEEE Fellow, AAAS Fellow and a Fellow of National Academy of Inventors.

Samar Saha
EDS Awards Chair

2019 IEEE EDS J.J. Ebers Award Winner

The 2019 J.J. Ebers Award, the prestigious Electron Devices Society award for outstanding technical contributions to electron devices, was presented to Professor H.-S. Philip Wong of Stanford University, Stanford, CA, USA, at the International Electron Devices Meeting in San Francisco, CA, on December 9, 2019. This award recognizes Professor Wong "For pioneering contributions to the scaling of silicon devices and technology".

H.-S. Philip Wong is Professor of Electrical Engineering at Stanford University since 2004. He holds the Willard R. and Inez Kerr Bell Professorship in the School of Engineering at Stanford University. From 1988 to 2004, he was with the IBM T.J. Watson Research Center. Since 2018, he has been on leave from Stanford to



H.-S. Philip Wong, 2019 IEEE EDS J.J. Ebers Award Winner and Fernando Guarin, 2019 IEEE EDS President

serve as Vice President of Corporate Research atTSMC, the largest semiconductor foundry in the world.

During his time at IBM, he conducted research on silicon transistors and image sensors, and managed exploratory research on high-k/metal gate, strained silicon, alternative channel materials such as Ge, multi-gate FET, FinFET, ultra-thin SOI, phase change memory—some of these early works have now become product technologies at various companies. At Stanford, his research aims at translating discoveries in science into practical technologies. His works have contributed to advancements in nanoscale science and technology, semiconductor technology, memory and logic devices, and electronic imaging.

Joachim N. Burghartz
2019 EDS J.J. Ebers Award Chair
Institute for Microelectronics Stuttgart
Stuttgart, Germany

IEEE ELECTRON DEVICES SOCIETY
J.J. EBERS AWARD

CALL FOR NOMINATIONS

The IEEE Electron Devices Society (EDS) invites the submission of nominations for the 2020 J.J. Ebers Award. This award is presented annually by EDS to honor an individual(s) who has made either a single or a series of contributions of recognized scientific, economic, or social significance to the broad field of electron devices. The recipient(s) is awarded a plaque and a check for $5,000, presented at the International Electron Devices Meeting (IEDM) or any one of the EDS's flagship conferences (EDTM, VLSI or PVSC).

Nominate:
J.J. Ebers Award
on-line nomination form:

https://ieeeforms.wufoo.com/forms/xl0lxns05xzwir/

Submission Deadline:
July 1, 2020

Contact:
If you have any questions regarding the EDS J.J. Ebers Award, please contact Laura Riello of the EDS Executive Office at l.riello@ieee.org

Visit:
https://eds.ieee.org/awards/j-j-ebers-award

ELECTRON DEVICES SOCIETY®

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Celebrating 125 Years
of Engineering the Future

2019 IEEE Electron Devices Society Education Award Winner

Professor Chennupati Jagadish

The EDS Education Award recognizes an IEEE/EDS Member from an academic, industrial, or government organization with distinguished contributions to education within the fields of interest of the IEEE Electron Devices Society. Professor Chennupati Jagadish was recognized at the IEEE Electron Devices Technology and Manufacturing (EDTM) Conference in Penang, Malaysia, March 16, 2020, as the 2019 EDS Education Award winner. The award cites Professor Jagadish "*For distinguished and sustained contributions globally to education, training and mentoring in the field of interest of the IEEE Electron Devices Society*."

Professor Chennupati Jagadish is a Distinguished Professor and Head of Semiconductor Optoelectronics and Nanotechnology Group in the Research School of Physics and Engineering, Australian National University. He has served as Vice-President and Secretary Physical Sciences of the Australian Academy of Science during 2012–2016. He is currently serving as President of IEEE Photonics Society, Past President of Australian Materials Research Society. Prof. Jagadish is an Editor/Associate editor of 5 Journals, 3 book series and serves on editorial boards of 19 other journals. He has published more than 920 research papers (640 journal papers), holds 5 US patents, co-authored a book, co-edited 17 books and edited 12 conference proceedings and 17 special issues of Journals. He won the 2000 IEEE Millennium Medal and received Distinguished Lecturer awards from IEEE NTC, IEEE Photonics Society and IEEE EDS. He is a Fellow of the Australian Academy of Science, Australian Academy of Technological Sciences and Engineering, The World Academy of Sciences, US National Academy of Inventors, Indian National Science Academy, Indian National Academy of Engineering, Indian Academy of Science, European Academy of Sciences, Andhra Pradesh Akademi of Science, IEEE, APS, MRS, OSA, AVS, ECS, SPIE, AAAS, FEMA, APAM, IoP (UK), IET (UK), IoN (UK), and the AIP. He received many awards including IEEE Pioneer Award in Nanotechnology, IEEE Photonics Society Engineering Achievement Award, OSA Nick Holonyak Jr. Award, Welker Award, IUMRS Somiya Award, UNESCO medal for his contributions to the development of nanoscience and nanotechnologies and Lyle Medal from Australian Academy of Science for his contributions to Physics. He has received Australia's highest civilian honor, AC, Companion of the Order of Australia, as part of 2016 Australia day honors from the Governor General of Australia for his contributions to physics and engineering, in particular nanotechnology.

Durga Misra
2019 EDS Education Award Chair
NJIT
Newark, NJ, USA

2020 EDS EDUCATION AWARD
CALL FOR NOMINATIONS

The IEEE Electron Devices Society invites the submission of nominations for the EDS Education Award. This award is presented annually by EDS to honor an individual who has made distinguished contributions to education within the field of interest of the Electron Devices Society. The recipient is awarded a plaque and a check for $2,500, presented at the IEEE International Electron Devices Meeting (IEDM).

The nominee must be an EDS member engaged in education in the field of electron devices, holding a present or past affiliation with an academic, industrial, or government organization. Factors for consideration include achievements and recognition in educating and mentoring students in academia or professionals in the industrial or governmental sectors. Specific accomplishments include effectiveness in the development of innovative education, continuing education programs, authorship of textbooks, presentation of short-courses at EDS sponsored conferences, participation in the EDS Distinguished Lecturer program, and teaching or mentoring awards.

Since this award is solely given for contributions to education, the nomination should exclude emphasis on technical contributions to engineering and physics of electron devices.

The nomination form can be found on the EDS website: https://eds.ieee.org/awards/education-award

The deadline for the submission of nominations for the 2020 award is September 1, 2020.

2019 IEEE Electron Devices Society Early Career Award Winners

The EDS Early Career Award recognizes young IEEE/EDS members who have made outstanding contributions in an EDS field of interest during the early years of their professional career after graduation.

The 2019 EDS Early Career Award was presented to the following young members: Luisa Petti of the Free University of Bolzano, Bolzano, Italy; Pragya Kushwaha of the University of California Berkeley, Berkeley, CA, USA and Qianqian Huang of Peking University, Beijing, China at the EDS awards dinner held in conjunction with the International Electron Devices Meeting in San Francisco, CA, on December 8, 2019.

Luisa Petti, Free University of Bolzano, Bolzano, Italy

Luisa Petti received her B.Sc. and M.Sc. in Electronic Engineering from Politecnico di Milano, Milan, Italy in July 2009 and December 2011, respectively. In February 2012 she joined the Wearable Computing Group at ETH Zurich, Zurich, Switzerland as a Ph.D. student to work on flexible oxide semiconductor thin-film transistors and circuits. In 2014, Luisa first spent six months at the Advanced Materials & Devices Group at Imperial College London, London, UK and then four months at the Emerging Display Technologies Group at Apple Incorporated, Cupertino, US. In June 2016 Luisa obtained her Ph.D. from ETH Zurich with a thesis entitled "Metal oxide semiconductor thin-film transistors for flexible electronics", for which she was awarded the ETH medal for outstanding doctoral theses. After a short post-doc at ETH Zurich, she joined first Cambridge Display Technology Ltd in October 2016 and then FlexEnable Ltd in December 2017 in Cambridge, UK as a research scientist. Since July 2018 Luisa is an Assistant Professor at the Faculty of Science and Technology at the Free University of Bolzano, Bolzano, Italy. Luisa's research interest includes the design, fabrication and characterization of a wide range of flexible electronic devices, ranging from sensors, energy harvesters and storage devices, to thin-film transistors and circuits based on both printing and micro-fabrication technique. Since 2012, Luisa has published 40 articles in prestigious peer-reviewed journals in the field including IEEE Transaction on Electron Devices, IEEE Electron Device Letters, IEEE Journal of the Electron Devices Society, IEEE Sensors, IEEE Sensor Journal, Nature Communications, ACS Nano, ACS Applied Materials and Interfaces, Applied Physics Review, Applied Physics Letters, Journal of Applied Physics, Advanced Materials, Advanced Functional Materials and Advanced Electronic Materials. The invited Applied Physics Review "Metal oxide semiconductor thin-film transistors for flexible electronics" she first-authored in 2016 has been cited more than 200 times. Other contributions include 30 proceedings at well-known international conferences in the field. In particular, Luisa has published 3 proceedings at the IEEE International Electron Device Meeting (IEDM), 2 of which she has presented as first author. Her presentation record includes 5 contributed presentations and 8 invited talks. According to Scopus (Google Scholar), her h-index is 20 (21) with a number of citations of 1206 (1531).

Luisa's early career also included two maternity breaks: one for her daughter Sofia (from July 2015 to January 2016) and the other one for her daughter Matilde (from October 2018 to March 2019).

Pragya Kushwaha, University of California Berkeley, Berkeley, CA, USA

With the advancement in technology, semiconductor industry faces new challenges every day with device performance and device-circuit co-optimization. SPICE modeling is the medium of information exchange from foundry to circuit designer. Dr. Kushwaha is currently involved in the development of industry standard compact models or SPICE (Simulation Program with Integrated Circuit Emphasis) models for emerging devices to be used in circuit design. These models are implemented in almost all the commercial simulators and used by IC chip designers as well as semiconductor foundries, like Apple, TSMC, Samsung, Intel, Qualcomm, Broadcom, GlobalFoundries etc. She is leading the efforts to develop Nanosheet Gate-All-Around FET, FinFET, FDSOI and PDSOI transistor models for digital, analog and RF circuit designs where the core is derived from Poisson's solution and short channel effects e.g. channel length modulation, velocity saturation, quantum mechanical effect etc. are added on top of the core. At high frequencies, the semiconductor device characteristics have frequency dependence via several inherent phenomena, like self-heating effect, substrate effect, and gate resistance effect. Hence, DC compact model is not sufficient to predict correct device behavior observed from measured data over a wide frequency range. Dr. Kushwaha addressed this issue and developed the physical understanding behind these frequency dependent phenomena. Dr. Kushwaha's research work in the field of sub-10nm semiconductor device modeling has influenced our daily life as the most advanced smartphones today in market have processor of 7 nm node FinFET process. Hisilicon's Kirin 970 SoC has used Dr. Kushwaha's research on RF-FinFET model in their process design kit. Healthcare devices like blood pressure measurement, heart rate measurement ECG machines etc. demand high precision, low frequency operated sensors. Dr. Kushwaha's research on low frequency noise model for advanced node FinFETs has been used by Qualcomm for their low power and low frequency circuit applications. The models developed by Dr. Kushwaha have been implemented in the industry standard models after comprehensive testing by several companies under the aegis of Compact Model Coalition. The proposed models have been successfully tested for various geometries including scalability, thus paving the way for future applications like next-generation communication network 5G and wearable gadgets. This is certainly a huge accomplishment given that the modern devices have very complicated architecture and needs a deep understanding of the physics, semiconductor device, as well as compact modeling technique.

Qianqian Huang, Peking University, Beijing, China

Qianqian Huang is an assistant professor at Peking University (PKU) in Beijng, China and selected as the Boya Young Fellow of PKU. She received her PhD. from the Institute of Microelectronics, PKU in 2015, and B.Sc. from the School of Electronic Engineering and Computer Science, PKU in 2010. Her research interests is in the area of emerging ultralow-power device technology for logic applications and neuromorphic computing, focusing on tunnel FET, negative capacitance FET and ferroelectric FET, and FET variability, reliability and noise. She has proposed and demonstrated the all-Si tunnel FETs through mechanism engineering with the state-of-the-art electrical behavior, and the novel tunneling technology of her work has been transferred to Semiconductor Manufacturing International Corporation (SMIC) and is being developed on standard foundry platform. She has also identified the physical mechanism of negative capacitance FET and presented its intrinsic conflict between switching and hysteresis optimization. More recently, she is working on the energy-efficient hardware implementation of artificial neurons for brain-inspired neuromorphic applications.

She has authored/co-authored more than 70 technical papers in international journals and conferences, including 10 IEDM and VLSI papers (6 papers as the first author, 3 papers as the corresponding author, 7 times as the presenter), and 11 EDL and TED papers, among others. She has applied more than 70 domestic and overseas patents, including 12 authorized US patents and 44 authorized Chinese patents. Her honors include the Forbes 30 under 30 in Science in China (2019), National Science Foundation of China for Excellent Young Scientists (2018), Young Talents of the L'Oréal-UNESCO For Women in Science Award in China (2017), Excellent Doctor Degree Dissertation Awards from the Chinese Institute of Electronics (CIE) (2016) and PKU (2015), Beijing Outstanding Graduates (2015), National Scholarship for graduate students from the Ministry of Education of China (2013, 2014), and Excellent Doctoral Graduate Academic Award from the Ministry of Education of China (2012). She is currently a member of the Board of Governors of the Women Scientist Association of CIE (2019-2021). She has served as the reviewer for a number of IEEE journals, including EDL, TED, J-EDS and TNANO, etc.

Meyya Meyyappan
2019 EDS Early Career Award Chair
NASA Ames Research Center
Moffett Field, CA

CALL FOR NOMINATIONS

2020 IEEE EDS Early Career Award

Description: Awarded annually to an individual to promote, recognize and support Early Career Technical Development within the Electron Devices Society's field of interest

Prize: An award of US$1,000, a plaque; and if needed, travel expenses not to exceed US$1,500 for a recipient residing in the US and not to exceed US$3,000 for a recipient residing outside the US to attend the award presentation.

Eligibility: Candidate must be an IEEE EDS member and must have received his/her first professional degree within the 10th year defined by the August 15 nomination deadline and has made contributions in an EDS field of interest area. Nominator must be an IEEE EDS member. Previous award winners are ineligible.

Selection/Basis for Judging: The nominator will be required to submit a nomination package comprised of the following:

- The nomination form that is found on the EDS web site, containing such technical information as the nominee's contributions, accomplishments and impact on the profession or economy and a biographical description.
- A minimum of two and a maximum of three letters of recommendation from individuals familiar with the candidate's technical contributions and other credentials, with emphasis on the specific contributions and their impacts.

The basis for judging includes such factors as: the demonstration of field leadership in a specific area; specific technical contribution(s); impact on the profession or economy; originality; breadth; inventive value; publications; honors; and other appropriate achievements.

Schedule: Nominations are due to the EDS Executive Office on August 15th each year. The candidate will be selected by the end of September, with presentation to be made in December.

Presentation: At the EDS Awards Dinner that is held in conjunction with the International Electron Devices Meeting (IEDM) in December. The recipient will also be recognized at the December EDS BoG Meeting.

Nomination Form: Complete the nomination form by August 15, 2020. All endorsement letters should be sent to l.riello@ieee.org by the deadline.

For more information contact: l.riello@ieee.org or visit: http://eds.ieee.org/early-career-award.html

Congratulations to the 28 Newly Elected IEEE Electron Devices Society Fellows

Effective January 1, 2020

Cor L. Claeys
2019 EDS Fellows Chair

Geoffrey Burr
for contributions to neuromorphic computing using non-volatile memories

Ting-Chang Chang
for contributions to non-volatile memory and thin-film transistor Technologies

Jiann-Fuh Chen
for contributions to power electronics in sustainable energy and high power systems

Pr Chidambaram
for contributions to strain engineering in MOSFETs and to designtechnology co-optimization

Chion Chui
for contributions to high-mobility germanium metal-oxidesemiconductor devices

Kukjin Chun
for leadership in microelectromechanical systems technology development

Thomas Crowe
for leadership in the development of terahertz devices and Instrumentation

Ravinder Dahiya
for contributions to tactile sensing

Barbara De Salvo
for contributions to device physics of nonvolatile embedded and standalone memories

Mool Gupta
for contibutions to laser material interactions

Muhammad Hussain
for contributions to flexible and stretchable electronic circuits

Benjamin Iniguez
for contributions to physics-based compact models of semiconductor devices

Akira Inoue
for development of inverse class-F power amplifiers for mobile phones

M Saiful Islam
for development of sensors and ultra-fast photodetectors

Martin Kuball
for contributions to Raman thermography in semiconductor devices

Gong-Ru Lin
for contributions to ultrafast fiber lasers and highspeed laser diodes for optical communications

Wallace Lin
for contributions to understanding transistor charging mechanisms

Po-Tsun Liu
for contributions to thin film transistor technologies

Kartikeyan Machavaram
for contributions to high-power millimeter wave and terahertz sources

Yiannos Manoli
for contributions to the design of integrated analog-to-digital interface circuits and energy harvesting systems

Durgamadhab Misra
for contributions to the reliability of CMOS gate stacks with high-k dielectrics

Bich-Yen Nguyen
for contributions to silicon on insulator technology

Shouleh Nikzad
for contributions to ultraviolet detectors for space applications

Byung-Gook Park
for contributions to charge trap flash memory and multiple patterning technology

Jae-Sung Rieh
for contributions to silicon-germanium integrated circuits for wireless communications

Steven Ringel
for contributions to compound semiconductor phototovoltaics

Ravi Todi
for contributions to innovative design and commercialization of high performance eDRAM

Laurence Tianruo Yang
for contributions to modeling and design for cyber-physical-social systems

Cor Claeys
2019 EDS Fellows Chair
KU Leuven, Belgium

EDS Members Recently Elected to IEEE Senior Member Grade

The IEEE Electron Devices Society would like to recognize the excellence of its valued members, especially when they have performed for a long time at a particularly high-quality level.

Congratulations to the following EDS members who have become IEEE Senior Members!

Ashok Bansiwal
Rongsheng Chen
Chris Deline
Joseph Friedman
Olusoji Ilori
Ziaul Karim
Andras Kis
Vadym Korotieiev
Chengkuo Lee
Kung-Yen Lee
Min Hung Lee
Gourab Majumdar
Maqsood Ali Mughal
Joyeeta Nag
Maria Nikolic
Mirko Poljak
Haroon Rashid
Biswajit Ray
Marco Rolandi
Murilo Romero
Shin-Ichi Takagi
Cedric Virmontois
Larg Weiland
Shu Yang
Ding Zhao

Do you know an outstanding IEEE member who is not yet an IEEE Senior Member?

Do you feel that you are qualified for such recognition?

Are you interested in becoming a Senior Member or nominating a fellow IEEE Member?

Visit the IEEE website for an application and for qualification requirements: https://www.ieee.org/membership/senior/

Heterogeneous Integration Roadmap (HIR) Event Resounding Success

By William Chen

The 3rd Annual Heterogeneous Integration Roadmap (HIR) meeting, Symposium and Workshop, held on February 20–21, 2020 at SEMI world headquarters, Milpitas, California, was a resounding success. The HIR is collaboratively sponsored by three IEEE Societies (EDS, EPS, Photonics) together with SEMI & ASME EPPD. The two-day event was held to celebrate the release of the HIR 2019 edition released on October 10, 2019 and to kick-off the preparation of the HIR 2020 edition. The HIR Symposium on February 20th featured presentations from all 22 Technical Working Groups (TWG), including a talk presented by EDS President Meyya Meyyapan on "Emerging Research Devices." They were complemented by two plenary speakers, Dr. Predeep Dubey from Intel Parallel Computing Lab spoke on "Virtuous Cycle of AI," and Dr. Hong Liu from Google Infrastructure spoke on "The Role of Optics on Computing." HIR Global Advisory Council members, Ajit Manocha gave the opening remarks in the morning, and Nicky Lu did the wrap-up in the afternoon. The TWG collaboration workshop agenda on February 21st started with a "Chiplet on the Rise Forum" with two speakers: Bapi Vinnakota from ODSA, and David Kehlet from Intel. This was followed by TWG collaboration sessions in preparation for the HIR 2020 edition. The total attendance of more than 180, included representatives from all 22 TWG teams as well as participation from a broad cross-section from the electronics industry, academia, government and research institutes, demonstrating the increasingly high interest and crucial relevancy in the Heterogeneous Integration Roadmap. This two-day event was sponsored by Google, Cisco, Intel, Promex, ASE Group, Samsung, Silitronics, together with SEMI and IEEE EPS, and co-organized by EPS Santa Clara Valley Chapter and SEMI.

Attendees of the HIR Workshop at SEMI

Download the Roadmap here: https://eps.ieee.org/technology/heterogeneous-integration-roadmap/2019-edition.html

Young Professionals Spain presents its "IEEE Inspiring Leaders" event at IEEE Day 2019

By Arturo Medina

During the weekend of October 11–13, 2019, the city of Valencia hosted the celebration of the traditional IEEE Day 2019 edition. However, this year this celebration had an even more special character, given that it was held in conjunction with the annual meeting of Region 8, that is, Europe, Africa and the Middle East. Therefore, we had the opportunity to immerse ourselves in the international spirit of IEEE, sharing venue and experiences with members from South Africa to Sweden.

Owing to this, a special atmosphere was continuously perceived during the meeting, because not every day one has the opportunity to attend in person the internal, complex but enormously interesting operation of a meeting of such a high level.

From Young Professionals Spain we wanted to capture the unique spirit of the occasion, looking for an activity that really did justice to the event. For this purpose, we wanted to emphasize the energy of the key members of IEEE, which through their continuous efforts make possible the work of this institution; they are the IEEE leaders, and they have the power to inspire both future generations and current members to continue their work in the organization, pushing it to achieve its goals and carry out its mission.

That is why we created the IEEE Inspiring Leaders event. For this we had the valuable collaboration of 5 IEEE leaders:

Distinguished leaders from the R8 chapters participated in the IEEE Inspiring Leaders event.

Through the discussions we tried to get answers to the questions what?, how?, and above all, why? standing behind the immeasurable value of the Leaders for IEEE.

There were four sections in which the questions were divided, each of which sought to approach a given aspect of the work of our participants:

- Inspiring Leadership.
- Your relationship with IEEE.
- IEEE as a volunteering activity.
- The future of technology.

In the first section we met different professional profiles of the collaborators, being able to witness the enormous variety of roles and tasks that can be performed in all engineering fields. Despite this diversity, everyone agreed on the main skills that an engineer must have, beyond their technical background, highlighting above all the capacity for collaboration

and communication with people from different disciplines.

In the second section we delved into the role that different members play within IEEE, and how they have reached this point. Most of them started as students, which highlights a fact that must always be kept in mind: the present, past and, above all, IEEE's future begins with the student members. It is essential to take care of them and keep them active and motivated.

Also in this section, the idea of how IEEE can benefit its members on a professional and personal level was reiterated. Of course, in all the cases IEEE has had an undeniable impact on the lives of our IEEE leaders, as this acronym is already an indelible element of their career.

Moving onto the third section, in which unfortunately we had to start reducing the number of questions, as time was pressing, we investigated how our participants organize their lives to achieve success in a professional career and at IEEE. Some ideas that were frequently mentioned were the need to have enough rest time dedicated to oneself, which requires having a clear organization and keeping in mind at all times what tasks you have to do in the short and medium term.

From right to left, the round table members were: Mona Ghassemian, Ana Cigarán, Maike Luiken, Péter Nágy and George Michael, accompanied by the moderator, Arturo Medina

Finally, we wanted to ask more open questions in the last section, seeking to know what they expect from the future. Key technologies such as renewable energy and its distribution, or more daring ones such as teleportation were discussed, as well as the great challenges of humanity, such as the elimination of plastics in our oceans.

Finally, we wanted to ask the participants what motivates them to move forward. In this sense, never stop enjoying what we do was an idea that arose, and to which we all agreed, as well as the self-imposed need to devote time to our personal development beyond our work.

Unfortunately, time was running out and we could not continue to enjoy the ideas of our speakers, which we could have been listening to and discussing for hours, given their great experience and, of course, their charismatic personality. It was a pleasure to have members so distinguished and yet so close. They showed us once again how IEEE is a community that not only has members of a very high technical level, but also has an open and charming people, always willing to lend a hand to anyone who needs help or advice.

We hope that this energy has served to inspire us all to continue our work at IEEE, and not let that spirit of effort and solidarity ever die.

IEEE YP Germany Social Meeting in Stuttgart

by Mike Schwarz

The IEEE YP Germany AG organized a social meeting in the Stuttgart metropolitan area, which was open for IEEE and non-IEEE members to attend. The meeting took place at the Burger House in the Stuttgart city center. Some nice conversations regarding past and future activities took place. It was a pleasant event for the new ExCom members of the IEEE YP Germany AG.

~Mike Schwarz, Editor

Sevda Adapour and Alan Blumenstein during the social meeting

Chapter News

MQ, DL and Conference Reports

COVID-19, How a Virus Affects the Science Community

By Mike Schwarz and Francis Balestra

Since mid of February, following approaching signs of COVID-19 pandemia, the organizers of the Joint Technical Meeting consisting of the MOS-AK Workshop, the Symposium on Schottky Barrier Devices and the IEEE DL MQ "Non-Conventional Technologies and Devices", have been discussing how to deal with the COVID-19 situation. First feedback of attendee's in our mail inbox was stating a cancellation of participation, because the risk was too high. We are observing the news regarding larger conferences, e.g. DATE, EuroSOI/ULIS, etc. DATE went virtual, EuroSOI/ULIS was finally postponed to the beginning of September.

In this situation we have reached the decision that we need to cancel the event. Due to very recent regulations no events gathering external attendees are allowed in the next few weeks. These rules are purely precautionary measures, which apply until April 30 and should help to minimize the infection risk. Several months of organization have been dissolved in the fog.

We contacted the MQ lecturers and arranged a new date in September or October. These are the good news, the game starts again. However, no one can predict the situation in half a year. We wish to hope for the best. We know how everyone feels in such situations. Looking at the present situation in China, where there are now only very few infections every day, a similar situation should happen elsewhere in the world, with a shift of time. Let's say for instance in Europe we think that in May the situation should be much better, therefore the conferences could be planned after summer vacation.

We also discussed having the conference virtually. But we decided against such a solution, because what makes conferences so attractive? These are networking, meeting friends, creating new collaborations, etc. They are missing in virtual events. Was it the right decision? We do not know, but we will see in autumn.

We know that the decision to cancel and/or postpone the event was the right solution at the moment we had to decide. Finally, we hope you all stay healthy and see you during the upcoming events.

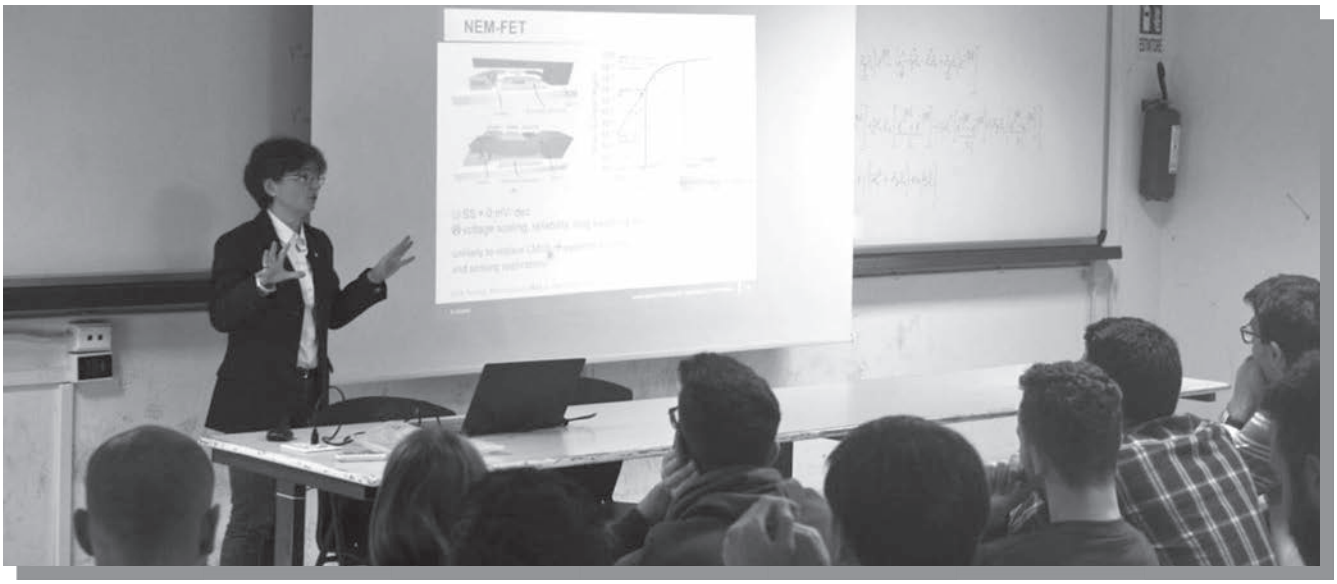
"Trends and challenges in Nanoelectronics for the next decade" by Elena Gnani

By Fernanda Irrera and Mike Schwarz

On December 2, 2019 the IEEE Electron Devices Society Distinguished Lecturer, Professor Elena Gnani of the University of Bologna gave a Lecture at the Department of Electronics Engineering of the Sapienza University of Rome (Italy).

The Lecture was entitled "**Trends and challenges in Nanoelectronics for the next decade**" and treated with nanoelectronics devices employed as a driving force for social applications and for a green sustainable world. Key fields such as security, energy, healthcare, transport, communication and infotainment are gaining more and more market so that microelectronics is becoming an inherent part of everyday life. The research related to nanoelectronics can be grouped in three main directions, i.e., More Moore, Beyond CMOS and More than Moore. Furthermore, general trends and challenges have been addressed in the Lecture.

The lecture started at 12:00 and lasted one hour. Approximately 60 persons attended the lecture, most



DL Elena Gnani during the lecture "Trends and challenges in Nanoelectronics for the next decade"

of which were Master class students and PhD Italian and foreign students. After the lecture, some questions were made to the DL regarding specific beyond CMOS devices and the perspective of arriving on the market.

The event ended approximately at 13:30.

~Mike Schwarz, Editor

"Silicon Carbide Device Technology for Power Devices and High Temperature Applications" by Mikael Ostling

By Fernanda Irrera and Mike Schwarz

Mikael Ostling, EDS Distinguished Lecturer

On November 8, 2019 the IEEE EDS Distinguished Lecturer Professor Mikael Ostling of the Royal Institute of Technology in Stockholm gave a lecture at the Department of Electronics Engineering of the Sapienza University of Rome (Italy).

The lecture was entitled "Silicon Carbide Device Technology for Power Devices and High Temperature Applications". The lecture discussed the properties of SiC as a semiconductor, and the current status of the technology for power devices/drivers and high temperature operation. Insights by examples of efficient SiC power devices capable of handling up to 20 kV breakdown voltage and integrated SiC devices capable of handling up to 500 °C were provided.

The lecture started at 3:15 pm and lasted one hour. Approximately 40 people attended the lecture, most of which were Master class students and PhD students. After the lecture, a lot of questions were made to the DL regarding the physics, the applications and the market of SiC and also some comments were made about the competitive role of SiC respect to GaN and Si itself. The event ended approximately at 5 pm.

In the next days, students were informing the professors that they had appreciated the lecture.

~Mike Schwarz, Editor

Prof. Victor Veliadis Distinguished Lecture

By Francis Balestra

On October 16, 2019, the IEEE Distinguished Lecture "SiC Power Devices and Applications" by Prof. Victor Veliadis, IEEE Fellow, Executive Director and CTO, PowerAmerica, Professor of Electrical and Computer Engineering, North Carolina State University, was held at IMEP-LAHC, Grenoble INP-Minatec. Within the lecture the attendees learned the importance of power electronics in an increasingly electrified technology driven world. Si power devices have dominated power electronics due to their low cost volume production, excellent starting material quality, ease of processing, and proven reliability. Si power devices continue to make progress but they are approaching their operational limits primarily due to their relatively low bandgap and critical electric field that result in high conduction and switching losses, and poor high temperature performance. The favorable material properties of Silicon Carbide (SiC) devices allow for highly efficient power electronic systems with reduced form factor and reduced cooling requirements. Emphasis has been placed on high impact application opportunities, including aerospace, automotive power electronics, grid applications, variable frequency drives for efficient high power electric motors at reduced overall system cost, and novel data center topologies with reduced cooling loads and higher efficiencies. Foundry considerations and design of SiC MOSFETs, currently being inserted in the majority of SiC based power electronic systems, has also been discussed. Cost reduction strategies has been outlined elucidating the path to the projected $1.5B SiC device market by 2023.

~Mike Schwarz, Editor

IEEE EDS Invited Lecture—ED Tsinghua University Student Branch Chapter

By Yancong Qiao

The ED Tsinghua University Student Branch Chapter held on November 19th an invited talk by Dr. Siyang Zheng of Carnegie Mellon University. In the talk entitled "Micro/nano engineering for medical diagnostics and chemical sensing" Dr. Zheng discussed first two latest endeavors of his group to isolate cell-released extracellular vesicles (EVs) and viruses for cancer diagnosis and virus discovery, respectively. In one approach they designed a nanomaterial, lipid nanoprobe (LNP), and an LNP-integrated microdevice to isolate EVs from blood plasma of cancer patients with high efficiency and speed. DNA mutations could be detected in the isolated EVs. Alternatively, they invented carbon nanotube (CNT)-integrated microfluidic devices for tunable size-based virus and EV isolation, followed by on-chip sample preparation. By applying this technology for environmental and clinical samples, they were able to successfully discover emerging viruses. Then, toward highly selective chemical sensing, Dr. Zheng's group has recently developed a high temperature MEMS flow control device to enable

Dr. Siyang Zheng's ivited talk on November 19th, for ED Tsinghua University Student Branch Chapter

chopper-modulated gas chromatography electroantennography (GC-EAG), an interesting new approach to detect volatile chemicals using insect antenna. The chopping operation significantly boosted the signal-to-noise ratio in an intrinsically noisy environment. Further development of this technology can provide a new approach for chemical sensing with ultra-high sensitivity and specificity.

IEEE EDS Distinguished Lecture—ED Beijing Chapter

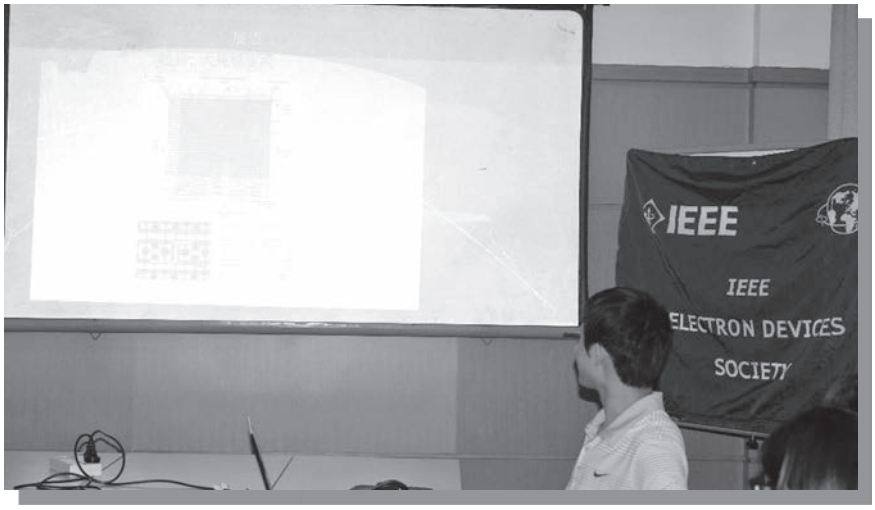
—by Kangwei Zhang

The ED Beijing Chapter held a DL talk on October 21 by Prof. Steve S. Chung, the Chair Professor of National Chiao Tung University. He gave a talk entitled "The Concept of Oxide-Breakdown Based PUF (Physical Unclonable Function) for Security in AI Era". First, the presenter discussed a concept of oxide-breakdown and its role for the understanding of how to generate an OTP (One Time Programming) memory for storage and/or security applications. Next, he introduced the concept to generate PUF. A breakdown mechanism discovered recently by Prof. Chung's group, especially on HKMG structures, can be used to develop not only OTP but also PUF. Then he demonstrated a novel concept of 2-bit-per-cell (2B/C) to realize a high-density OTP PUF from a new scheme of the dielectric breakdown. Finally, he addressed possible applications to system security. About 30 attendees and several professors attended this talk. 30 researchers and several professors attended this Distinguished Lecture.

IEEE EDS Invited Lecture—EDS UCAS Shanghai Student Branch Chapter

—by Binbin Pei

In order to provide a platform to learn from each other, and improve our presentation skills, an Academic Salon was held every Tuesday, from September 9, 2019 to January 14, 2020, hosted by EDS UCAS Shanghai Student Branch Chapter. We were inviting doctoral and graduate students from the State



EDS UCAS Shanghai Student Branch Chapter

Prof. Steve S. Chung DL on October 21st for ED Beijing Chapter; Speaker (1st row, 4th from right) with the audience

Key Laboratory of sensor technology to share their research experience and academic achievements. In addition, this Academic Salon was inviting experts from MEMS academia and industry to make special invited reports. On December 16, 2019, Mr. Wang Yi, CEO of MEMS Consulting Company, was invited to make a report on MEMS market and industrialization.

IEEE EDS Invited Lecture—ED Yeongnam (Taegu) Chapter

—by Chang-Ki Baek

On November 20, 2019, the IEEE Region 10 seminar was held at Pohang University of Science & Technology (POSTECH) with invited Distinguished Lecturers Prof. Jin-Woo Kim, a Director of Bio/Nano Technology Group at University of Arkansas, and Prof. John T.W. Yeow, a Director of Advanced Micro/Nanodevices Laboratory at the University of Waterloo.

At the 1st session, Prof. J.-W. Kim gave a talk on "Programmable Molecular/Nanoscale Building Blocks and Development Strategies for Multifunctional Hybrid Soft Nanomaterials in Bio/Nano Medicine." In this lecture, Prof. J.-W. Kim presented the progress in and challenges to the controlled assembly of nanoparticles (NP) into structures with specific shape and function. He also discussed the "programmable and customizable" integrations of highly functional bio-hybrid systems in desired patterns and geometries, and drive innovations in the novel hybrid fused technologies, particularly for in vivo, real-time molecular/nano imaging and sensing in medicine.

Consequently, at the 2nd session, Prof. J.T.W. Yeow gave a lecture "Highly Miniaturized Biomedical Imaging Devices." This lecture was focused on micromachining technology and nanomaterials in the field of biomedical instrumentation, and on current development of miniaturized x-ray CT machines, and ultrasound imaging devices in the Advanced Micro/Nanodevices Laboratory at the University of Waterloo. The speaker emphasized that the small size and low mass provided by micro/nanodevices make medical instruments portable, power-efficient, and, in many cases, more effective.

This event was organized by the ED Yeongnam (Taegu) Chapter. A technical support for this seminar was provided by Pohang University of Science & Technology (POSTECH).

~Ming Liu, Editor

Prof. J.-W. Kim and Prof. J. T. W. Yeow's invited talks on November 20th for ED Yeongnam (Taegu) Chapter

Regional News

USA, Canada & Latin America (Regions 1-6, 7 & 9)

ED/SSC Recife Chapter, Natal, Brazil

—by Vincent Bourguet

EMicro-NE (Escola de Microeletronica do Nordeste) is an event held annually in the Northeast of Brazil, as an introduction to Microelectronics for undergraduate students, aiming to contribute to education and motivate students for the field of electron devices and integrated circuits. The 14th edition was held this year on November 15 and 16, in the city of Natal, capital of the state of Rio Grande do Norte. The event was composed of a series of twelve minicourses and two invited talks: https://emicrone.ect.ufrn.br/index.php

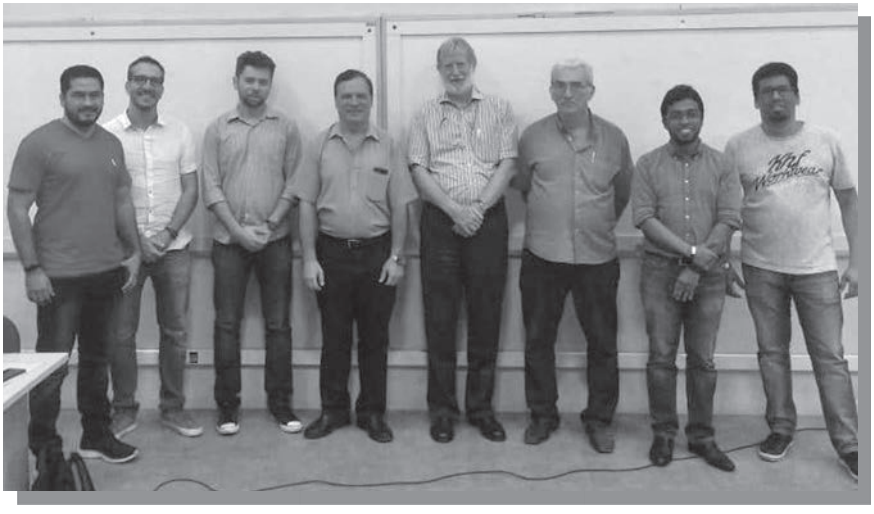
The invited talks were delivered by two EDS Distinguished Lecturers: Jacobus Swart and João Antonio Martino. The titles of these two talks were respectively: "Innovation by ASIC design and Related Electron Device Issues" and "Evolution and Applications of Micro/Nanoelectronics." The lectures were attended by over 60 people each.

This year a request for partial funding of the EMicro-NE school by EDS was submitted and approved for the first time. The event had free registration for students and received some support from the organizing universities, such as the venue, lodging and transport of students from other universities in the region.

250 students attended the school. They were all very enthusiastic about the contents and learning during the event. Good results are seen along many years of the EMicro-NE school,, because many participants followed afterwards with graduate studies in the microelectronics area and some of them became academics at the local universities.

An additional, though important outcome of the event is a promotion of EDS, aiming to disseminate a knowledge about the Society goals and activities and to increase the EDS member community in the region.

~ Edmundo Guiterrez, Editor



DL's and organizing committee, from left to right: Wallace Pimenta, Vincent Bourguet, Francisco Vidal, João Martino, Jacobus Swart, Raimundo Freire, Gutenberg dos Santos Jr. and Bruno Leonardo

Europe, Middle East & Africa (Region 8)

Experts gathered in Aachen to discuss the challenges of wafer-scale integration of graphene and 2D materials

—by Frederica Haupt

In the past ten years, graphene and other two-dimensional (2D) materials have allowed prototyping devices with exceptional performances and a potentially huge impact in electronics, photonics and sensor technology. Success in real-world applications requires, however, not only outstanding performances at the single-device level, but also mass-production processes. The next big challenge in the field is therefore the development of large-scale fabrication processes ideally compatible with conventional silicon technology. This challenge has been the topic of a workshop that took place in Aachen on November 12–13, 2019.

The workshop has been organized by Daniel Neumaier (AMO GmbH) and Max Lemme (AMO GmbH & RWTH Aachen University) within the

Participants of the Wafer-Scale Integration Workshop of 2D materials

framework of the Aachen Graphene and 2D Materials Center. It counted about 100 participants, including many leading experts from European industry and academia. "Devising strategies to integrate 2D materials into conventional electronic devices is an effort that requires input from very many perspectives", says Neumaier. "Two days of open exchange with colleagues and friends like the ones we just had in Aachen are always a good source for new ideas, motivation and collaborations."

The workshop has been financially supported by the European Union via the projects G-IMAGER, QUEFORMAL, ORIGENAL and ULISSES, and by the German BMBF via the projects GIMMIK and NOBLENEMS.

DL Prof. Benjamin Iniguez during the distinguished lecture on Schottky Barrier MOSFETs

Benjamin Iniguez Distinguished Lecture on SB-MOSFETs device physics and modeling aspects

—by Mike Schwarz

Within the time frame of the 3rd Symposium on Schottky barrier MOS devices on October 4, 2019, at the Amphi Bloch of CNRS in Paris, Prof. Benjamin Iniguez (DEEEA, Universitaet Rovira I Virgili) gave a distinguished lecture on Schottky Barrier MOSFET devices.

The lecture was focused on the device physics, in particular on how to model these devices, what are the key physics issues to be modeled, and what models are present available. The lecture was well attended by 20 IEEE participants and approximately 10 non-IEEE members.

Remembering Jan Czochralski

—by Mike Schwarz

One of the most important technological discoveries of the 20th century is known only to insiders. That it was invented in Oberschöneweide (Berlin, Germany) by Jan Czochralski, a plaque on the campus Wilhelminenhof of the HTW Berlin helps to recognize since 15th November 2019. The plaque is dedicated to Jan Czochralski.

Jan Czochralski was born in Poland and was a successful researcher in Germany. By a "strange coincidence" more than 100 years ago, working in the metal laboratory of Kabelwerk Oberspree of AEG he drew the first single crystal from a liquid tin. The process based on this invention is still used to produce silicon monocrystals and has become the basic technology of the digital age. Almost half of all solar cells installed worldwide today are made of monocrystalline silicon produced using the Czochralski process. Czochralski's invention makes a huge contribution to climate protection and contributes to the rapid development of the chip industry, which significantly shapes our everyday lives. Just think of smartphones and microprocessors.

Ceremony of Jan Czochralski plaque in Berlin by IEEE Poland and Germany Sections

This was a reason for IEEE Poland and Germany sections to jointly acknowledge in 2019 the importance of the invention by Jan Czochralski in the form of the "Milestone Event Warsaw—Kcynia—Berlin". More details of this Milestone are available at the website https://ethw.org/Milestones:Czochralski_Process.

Symposium on Schottky barrier MOS devices "Towards neuromorphic and quantum computing applications"

—by Mike Schwarz, Laurie Calvet and John Snyder

The 3rd Symposium on Schottky barrier MOS devices was held on October 4, 2019 at the Amphi Bloch, Orme de Merisiers-CEA, Gif-sur Yvette, France. It was sponsored by LabEx Nanosaclay, the ED France Chapter, IEEE Young Professionals Germany Affinity Group, Silvaco Europe Ltd., Robert Bosch GmbH and hosted by Drs. Laurie E. Calvet and Francesca Chiodi (Center of Nanoscience and Nanotechnology, CNRS-Université Paris-Sud). It was attended by 25 IEEE members, with approximately 10 non-IEEE members.

The symposium started with a welcome breakfast at Amphi Bloch and introduction of the attendees. Afterwards, Prof. Benjamin Iniguez (DEEEA, Universitaet Rovira I Virgili) gave a distinguished lecture on Schottky Barrier MOSFET devices concentrating on the device physics with a special focus on modeling.

After a discussion and coffee break, the symposium continued with an inspiring retrospective starting with the work of Walter Schottky in the late 1930s, followed by a review of the current state of the art on SB-MOSFET technology by Dr. John Snyder (JCap, LLC). Afterwards, Dr. Philippe Blaise (Silvaco Inc., France) explained the new atomistic simulation functionality of the Silvaco tool chain, especially for applications concerning 2D materials and the semi-quantitatively extraction of specific resistances of metal-semiconductor interfaces. The morning session ended with a presentation by Dr. Radu Sporea (Surrey, UK) about TFT transistors, the possibility of using source gating and its ability to realize very high gain and increased power-efficiency.

The afternoon session began with a presentation by Dr. Satender

Dr. Satender Kataria during the talk Graphene/Si Schottky diodes and participants

Some participants of the Symposium on Schottky Barrier Devices 2019

Kataria (RWTH Aachen, Germany) on Graphene/Si Schottky diodes and the impact of quantum efficiency of photondetectors. Next, Prof. Denis Flandré (UC Louvain, Belgium) provided a detailed and thorough impressive investigation on the figures of merit of cryogenic nanoscale transistors, with the idea of using them for quantum computing applications. Dr. Francesca Chiodi (C2N, CNRS-Université Paris-Sud) then gave an overview on how laser doping using excimer lasers can be used to realize superconducting silicon and a discussion of all silicon Josephson junctions. Next, Dr. François Lefloch (CEA, Grenoble) provided an overview of how SB-MOSFETs can be turned into Josephson junctions for quantum computing applications when the PtSi silicide becomes superconducting below 1K. The quantum computing section then concluded with a very clear seminar by Dr. Fabrice Nemouchi (CEA, Grenoble) on Qubits using SB-MOSFETs. He referred to engineering of the metal-semiconductor interface, spin qubits and technology aspects e.g. annealing impacts in metal-semiconductor interfaces.

The last two talks on neuromorphic applications were given by Dr. Laurie Calvet (C2N, Palaiseau, France) and Dr. Mike Schwarz (Robert Bosch GmbH, NanoP THM, Germany). After an introduction to neuromorphic hardware, Dr. Calvet discussed why SB-MOS devices have advantages over conventional devices. Afterwards, Dr. Schwarz closed the symposium with his talk on SB-MOS device modeling and its application to neuromorphic computing, focusing on how to extract important characteristics from device simulations for the optimization of neuromorphic circuits.

32nd Bipolar Working Group (AKB) Workshop, STMicroelectronics, Crolles

—by Tommy Rosenbaum

The 32nd AKB Workshop took place on November 14–15, 2019, at the facilities of STMicroelectronics in Crolles, France. Initially, the "Arbeitskreis Bipolar" (AKB) started off as an industry-oriented compact modeling workshop dating back to 1986. As a remnant, the original name still relates to the German-speaking roots. At the time, the "Institut für Mikroelektronik Stuttgart" led the group as a neutral institution within a group of industry members. Over time, more and more companies and institutions from all over Europe joined and expanded the yearly meeting. In 2000, Infineon Technologies AG ("Siemens Halbleiter" before) took over the responsibility and has been chairing the working group till this day.

Participants of the 32nd AKB Workshop

Even though the AKB is still a bipolar transistor focused workshop (this year, slightly over half of the presentations were BJTs/HBTs related), the decision was taken in 2015 to widen the topics to all device types. In comparison to other conferences and workshops, the AKB is focused more on concrete applications and also tackles issues faced by daily compact modeling. This is taken into account by additional discussion slots appended to the actual presentations.

Looking at the statistics, over 200 presentations were given since the beginning of AKB – of which one third concentrated on generic modeling, followed by 25% of actual compact model development (HICUM, HiSIM, diode CMC, etc.) and 15% of parameter extraction. Most of the remaining portion can be attributed to measurements, technology and simulations/simulators.

This year, the workshop was organized in two parts: the second day was dedicated to bipolar transistors only, whereas the first day had no specific focus and addressed generic modeling topics instead. Next year, our new member Rohde & Schwarz will host the meeting in Munich on November 19th and 20th. Until then, the interested reader may refer to the publicly available presentations online:

https://www.iee.et.tu-dresden.de/iee/eb/forsch/AK-Bipo/ak_bipo_bei.html

Executive Committee Meeting of IEEE Germany Section

—by Sevda Abadpour and Mike Schwarz

The IEEE ExCom Germany organized an annual meeting in Frankfurt from October 24th–25th. The host was VDE-Haus in Frankfurt/Main. During the meeting, each committee and student branch reported past activities during the last year and the planning for 2020. Also, Sevda Abadpour from IEEE Young Professional Germany committee participated in the ExCom meeting and presented the reformed YP Germany group.

The ExCom committee presented the result of the IEEE R8 meeting, which was held October 11th–13th. The IEEE Germany ExCom has introduced the IEEE Learning Network (https://iln.ieee.org/public/Training

Participants of the Executive Committee Meeting of IEEE Germany Section

Catalog.aspx) which is the place for IEEE membership to find IEEE continuing education. There was more discussion about the reporting by every committee about their activities in IEEE vTools. Additionally, potential chapter opportunities were presented. To summarize, it was a great event for the YP Germany AG, especially by participating and communicating with other committees.

~ Mike Schwarz, Editor

Recent activities of the IEEE Ukraine Section (East) AP/MTT/ED/AES/GRS/NPS Societies Joint Chapter

—by Dr. Kateryna Arknypova and Ms. Daryna Pesina,
IEEE Ukraine Section (East) Joint Chapter Chairperson and Secretary (2019-2020)
http://www.rocket.kharkov.ua/~euachapter/

The First IEEE Milestone in Ukraine to celebrate "Zenit Parabolic Reflector L-band Pulsed Radar 1938" in Kharkiv

On November 21, 2019, a commemorative plaque recognizing the IEEE Milestone "Zenit Parabolic Reflector L-band Pulsed Radar 1938" was finally unveiled at the School of Radiophysics, Biomedical Electronics and Computer Systems (SRBECS) of the V. N. Karazin Kharkiv National University (KhNU).

The Zenit radar was designed at the Ukrainian Institute of Physics and Technologies by a group of prominent microwave scientists led by Abram Slutskin and his former students Oleksandr Usikov and Semion Braude. The first successful field test of Zenit, two-parabolic-antenna L-band pulsed radar, was performed in Kharkiv on October 14, 1938. It demonstrated the ability to determine accurately all three coordinates of a flying airplane, whereas at that time all the existing systems were able to determine only two coordinates of airborne targets. Zenit had a skillful combination of two principal innovations: it was using pulsed method and was working with waves of the 60-65 cm wavelength, i.e. shorter than commonly used before.

The ceremony gathered many Ukrainian scientists and engineers, IEEE representatives and volunteers: Prof. Jan Machac, IEEE MTT-S Region 8 coordinator, Prof. Vil Bakirov, rector of KhNU, Prof. Petro Melezhik, director of IRE NASU, Prof. Vyacheslav

IEEE Milestone Plague "Zenit Parabolic Reflector L-band Pulsed Radar 1938"

IEEE Milestone unveiling ceremony: Prof. F. Yanovsky is speaking

Prof. J. Machac (the third from the right) and members of IEEE from the Ukrainian research community at the IEEE Milestone plaque

Zakharenko and Prof. Leonid Litvinenko, present and former directors of IRA NASU, respectively, Prof. Felix Yanovsky, IEEE Fellow and IEEE Ukraine Section vice-chair, Mr. Ievgen Pichkalyov, IEEE Ukraine Section chair, and others.

In his welcome address, Prof. F. Yanovsky noted, "Out of almost 200 IEEE milestones worldwide, only six have been granted to the developments of radar technologies, and one of them is now located in Ukraine. This was a huge achievement and today this is a great honor."

Following the unveiling ceremony, Prof. A. Nosich delivered a lecture on the work of the Zenit radar inventors. The event was finished with a small welcome reception organized by IEEE Ukraine Section and its Kharkiv subunits.

~ Kateryna Arkhypova, Editor

Asia & Pacific (Region 10)

IEEE CAS/ED/SSC Wuhan Chapter and Huazhong University of Science and Technology Organized a Technical Talk

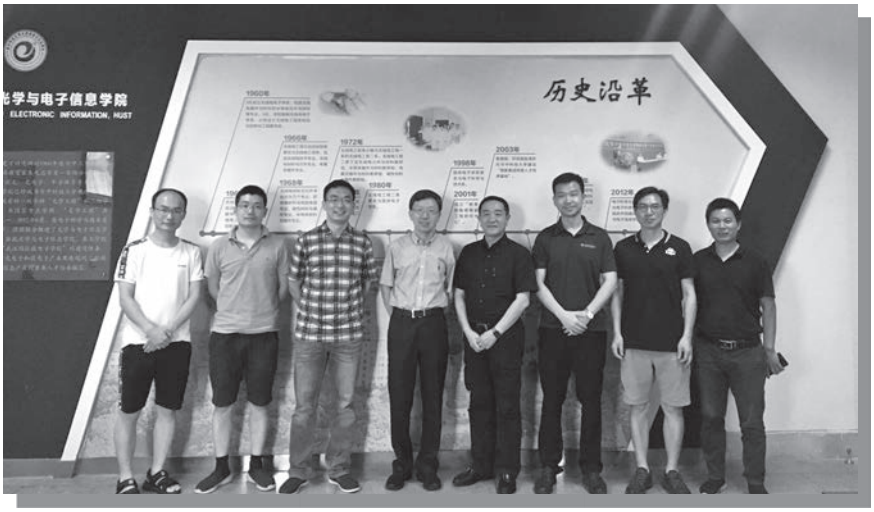
—by Chao Wang

The IEEE CAS/ED/SSC Wuhan Chapter, along with the School of Optical and Electronic Information, Huazhong University of Science and Technology (HUST), China, held a technical talk by Professor Yong Ping Xu of National University of Singapore on 23 July 2019. Prof. Xu's talk was entitled "Implantable Medical Devices—Interface with the Human Nervous System". This was the first-time SSCS technical event held in the campus of HUST, after the formation of the joint chapter was approved in early July 2019.

Prof. Xu began with a brief introduction on the history of implantable medical devices that interface with the human nervous systems. First, Prof. Xu highlighted the commercialized devices which have been widely used in various medical applications, e.g., implanted cochlear and pacemaker. Then, he also discussed the advanced devices being developed for emerging applications, such as neural recoding and stimulating devices for treating neurological problems caused by nervous system disorder or injury. Prof. Xu introduced the principle of human nerve cells and explained the generation and transmission of the nerve signals. By discussing a few case studies of cutting-edge implantable medical devices, he explained how to use advanced microelectronic technology and integrated circuit design to record neural signals and stimulate nerve cells with high efficacy. Prof. Xu introduced, how a system-on-chip (SOC) device is designed to be capable of altering the neural activities through neuromodulation, and hence performing neurotherapy and nerve repair, or acting as a neuroprosthesis. He explained the design approach of some exemplary circuits including neural recording amplifiers and electrical simulator circuits developed by his team at the National University of Singapore (NUS). These novel circuit solutions were discussed thoroughly, to explain how to address the stringent challenges in the neural interface design, such as ultra-low noise, high input impedance, large input dynamic range and low power consumption for neural recording amplifiers, sufficient stimulation strength with high efficacy and safety complaint for electrical stimulators.

The audience enthusiastically listened to the talk, asked many

Prof. Yong Ping Xu's talk "Implantable Medical Devices—Interface with the Human Nervous System," Huazhong University of Science and Technology (HUST), Wuhan



Prof Yong Ping Xu with the organizers from HUST after the lecture (From left): Dr. Min Run, Dr. Xiaojun Bi, Prof. Benpeng Zhu, Prof. Yong Ping Xu, Prof. Xuecheng Zou, Prof. Chao Wang, Dr. Zhige Zou, and Dr. Guoyi Yu

questions triggering interactive discussions, during which Prof. Xu gave very thoughtful answers and provided an insight to the brain-machine interface system designs in the future.

Bingqiang Liu, a Year-3 undergraduate from HUST, said "Prof. Xu taught us how to design appropriate stimulation circuits to enable people to regain control of the limbs for the broken human nerves. From the lecture, we can see many scientific problems and technical challenges in the fields of biomedical circuits and devices. Prof. Xu's talk is meticulous and inspiring, which makes me touch the cutting-edge research field and technology direction in the solid-state circuit designs." Another undergraduate, Qirun Hong, said, "From the lecture, I was quite surprised to see the similar circuit structures with those in the CMOS analog integrated circuit design textbooks. It can be seen that many classical circuits we have learned in the undergraduate classes are still practical in the actual design and still have great potential. I believe that operational amplifiers, as the basis of analog circuits, will continue playing a very important role in the design of advanced analog circuits for many emerging applications!"

~ Ming Liu, Editor

IEEE CAS/ED/SSC Wuhan Chapter Held Opening Ceremony and Organized Advanced Integrated Circuits Forum

—by Chao Wang

On 10 October 2019, an opening ceremony was held at the campus of Huazhong University of Science and Technology (HUST), Wuhan, China, to celebrate the formation of the IEEE CASS-EDS-SSCS Wuhan Joint Chapter (Wuhan Joint Chapter). The opening ceremony was organized together with a technical forum on advanced integrated circuit (IC) and an advanced IC poster competition for students. The event was jointly hosted by the Wuhan Joint Chapter, the School of Optical and Electronic Information (SOEI), and the Wuhan International Institute of Microelectronics (WHIME), HUST.

In the morning session, Prof. Jiang Tang, the dean of SOEI, HUST, firstly delivered an opening address and congratulated the formation of the Wuhan Joint Chapter. He talked about the important role of the Joint Chapter and how it will help the faculty and students to advance their careers in either academia or industry. Next, Prof. Chao Wang, the founding chair of the Chapter, from HUST, introduced the newly-established Chapter. Specifically, he introduced the newly-formed committee from eight founding organizations including the HUST, Wuhan University, Hubei University, Hubei University of Technology, XMC, Synopsys Wuhan Limited, Tianma Microelectronics, and FiberHome Microelectronics. Then, on behalf of IEEE, Prof. Yong Lian, the President of IEEE CAS Society, officially announced the formation of the IEEE CASS-EDS-SSCS Wuhan Joint Chapter and awarded the Chapter Banner to the Chapter Chair, Prof. Chao Wang.

Afterwards, Prof. Guilin Zheng, the Chair of IEEE Wuhan Section, from Wuhan University, introduced the IEEE Wuhan Section and the IEEE Region 10. He talked about the benefits of IEEE membership including the access to IEEE publication, professional networking, career opportunities, continuing education, etc. Then, Prof. Yong Lian, the IEEE CASS President introduced IEEE and promoted the CAS Society. He encouraged the faculty and students to join the IEEE and its affiliated societies and participated in the various IEEE-sponsored activities around the world. Prof. Yoshifumi Nishio, the Vice President of IEEE CAS Society, from Tokushima University, spoke next to promote the CASS. Prof. Nishio introduced the activities of CAS Society in Region 10 and encouraged the students to join the CAS Society on the spot. Following the CASS representatives, Dr. Shuji Ikeda, a BoG member of IEEE ED Society, promoted the IEEE ED Society by introducing the society and its regional activities in Region 10. Prof. Hanjun Jiang, the former chair of IEEE SSCS Beijing Chapter, from Tsinghua University, promoted the IEEE SSC Society and also shared the growing experience of the SSCS Beijing Chapter to the newly-formed Wuhan Joint Chapter. As the Vice Chair of an outstanding chapter of the IEEE CAS Society, Dr. Kwen-Siong Chong from CASS Singapore

A group photo of the newly-formed IEEE CASS-EDS-SSCS Wuhan Chapter

Chapter also shared the success experience by introducing the chapter organization and activities in the past few years.

The afternoon session was the advanced integrated circuit forum consisting of five technical talks. Firstly, Prof. BahHwee Gwee, the committee member of CASS Singapore Chapter, from Nanyang Technological University, gave a talk on machine learning for automatic analysis of delayered IC images. Then, Prof. Guoxing Wang, the Vice President of IEEE CAS Society, from Shanghai Jiaotong University, gave a lecture titled "A New Signal Processing Paradigm: Continuous-Time Discrete-Amplitude (CTDA) Systems". Afterwards, Prof Runsheng Wang, from Peking University, gave a talk titled "The Smaller, the Bigger—Understanding Variability in Nanoscale CMOS Devices and Circuits". Prof. Chun Zhang, from Tsinghua University, talked about sensors and integrated circuits for robots. Finally, Prof Qiang Li, the Chair of CASS Chengdu Chapter, from University of Electronic Science and Technology, talked about ultra-low voltage ADC design.

The one-day event was concluded by the award ceremony of the advanced IC poster competition. In total, there were 19 students from various universities (HUST, Wuhan University, Hubei University of Technology, and Nanyang Technological University, etc) who had submitted a poster to present his/her research work in the fields of integrated systems, circuits and devices. All posters were assessed by a panel of six professors through one round of online examination and another round of assessment in the poster session during a tea break. Based on the scores of the panel members, the first-class, second-class, and third-class winners received award certificates and cash prizes. The results of the competition are as follows:

One first-class prize (RMB 500): Zhicheng Wang, "A Time-Division-Multiplexing (TDM) Scheme for Simultaneous Wavelength Locking of Multiple Silicon Micro-rings";

Two second-class prizes (RMB 300 each): Nian Duan, "An Electro-Photo-Sensitive Synaptic Transistor for Edge Neuromorphic Visual System"; Yi Zhan, "A 180nW 100KHz ultra-low power relaxation oscillator."

Three third-class prizes (RMB 100 each): Jia Chen, "A Comprehensive Mixed Hardware-Software Study on 1T1R RRAMs based Convolution Neural Network"; Kaixuan Ye, "A 0.5-V Capless LDO with 30-dB PSRR at 10-kHz Using a Lightweight Local Generated Supply"; Long Cheng, "Functional demonstration of in-memory arithmetic logic unit in memristive crossbar array".

About 100 research faculty and students attended the opening ceremony and technical forum. The event was well received and very successful.

Wuhan the biggest city in the central China, is famous as the one of the four key semiconductor bases as well as one of the higher education hubs in China, which has many famous semiconductor companies and more than 80 universities. The Wuhan Joint Chapter plans to build a platform for the academia and industry in Wuhan area in the field of integrated circuits, and also to help to promote academic exchanges between Wuhan and the rest of the world.

~ Ming Liu, Editor

ED Malaysia Kuala Lumpur Chapter

—by S.N. Ibrahim, H. Mamat, & N. Soin

IEEE EDS Malaysia Membership Drive at IEEE Open Day 2019 at MAGIC Cyberjaya

This programme was executed at MaGIC (Malaysian Global Innovation and Creativity Centre) Cyberjaya on

IEEE Malaysia Open Day 2019 Photo Session

12 October 2019 and was attended by about 100 participants. The event was organised by the IEEE Malaysia Section and EDS Malaysia Chapter as co-sponsors. The membership drive was carried out in conjunction with the IEEE Day 2019 celebration and IEEE Malaysia Section Student Congress 2019. There were a few activities conducted on the day such as Town Hall Session, Malaysia Distinguished Lecturer Program (MyDLP), Senior Membership Workshop, Teacher In-Service Program, Student Congress, Humanitarian Activities Sharing session and the ceremony for IEEE Malaysia Section Final Year Project (FYP) Award. During the event, the representatives of the IEEE Malaysia Section took the opportunity to display the new logo of the Section. About 300 participants joined the event on the day. Many participants were eager to know more about IEEE and EDS Chapter. The attendees were mostly students, school teachers, lecturers and industry experts.

Participants at the technical talk (Prof. Wing Cheung Mak standing in the middle)

Technical Talk: Advanced Design and Fabrication Strategies to Improve Biosensor Performance at University Malaya

In collaboration with the University of Malaya and the International Islamic University Malaysia, the IEEE EDS Malaysia Chapter conducted a Technical Talk on "Advanced Design and Fabrication Strategies to Improve Biosensor Performance". The talk was given on the 15 October 2019 by Assoc. Prof. Wing Cheung Mak (Martin), the Head of Biosensor and Bioelectronics Unit, Linkoping University, Sweden. About 15 participants attended the talk and derived an immense knowledge from the presentation.

~ P. Susthitha Menon, Editor

EDS Vision, Mission and Field of Interest Statements

Vision Statement
Promoting excellence in the field of electron devices for the benefit of humanity.

Mission Statement
To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition and enhancing public visibility in the field of Electron Devices.

EDS Field of Interest
The EDS field-of-interest includes all electron and ion based devices, in their classical or quantum states, using environments and materials in their lowest to highest conducting phase, in simple or engineered assembly, interacting with and delivering photo-electronic, electro-magnetic, electromechanical, electro-thermal, and bio-electronic signals. The Society sponsors and reports on education, research, development and manufacturing aspects and is involved in science, theory, engineering, experimentation, simulation, modeling, design, fabrication, interconnection, reliability of such devices and their applications.